DESIGN AND ANALYSIS OF ULTRASONIC NDT INSTRUMENTATION THROUGH SYSTEM MODELING

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Abstract

System modeling techniques were used to perform a power analysis of a battery-operated non-destructive testing system to reliably predict the required power source for the system. Topology-specific and equivalent circuit models written in SPICE were employed for modeling this multi-engineering discipline system. Crucial system constraints such as power consumption and power dissipation were simulated and evaluated. Presented here is the modeling work carried out on the electromechanical load, excitation-circuits and high-voltage power supply. Simulation schematics were translated into hardware schematics and prototyped. Measurements on prototyped hardware are also presented for comparison with simulation results and model evaluation. Close mapping of simulation results to real hardware was obtained for topology-specific models; agreement within 20% was achieved for equivalent circuit models. The system model developed in this study is currently being used as a virtual test platform for verifying various design methodologies and foreseeing uncertainties.

Introduction

Structures which are installed and operate in harsh environments in extreme conditions are likely to fail prematurely. Reliable structural monitoring instrumentation is crucial for monitoring the condition of these structures. Long Range Ultrasonic Testing (LRUT) is a novel non-destructive testing (NDT) method used in the detection of volumetric defects such as gross corrosion [1].

The LRUT method uses elastic waves (sound waves) in the kilohertz range and allows couplant-free transducer coupling to the test specimen. In LRUT, a pulse-echo method is often used so that access to a single location is enough to inspect long range. The A-Scan (top) and its corresponding A-Map of a pipeline being inspected on both sides from a single test location are shown in Figure 1. A-scans are plots of signal amplitude against time and A-Map is the plan view of the pipe length. In this method, a transducer or an array of transducers excites sound waves, which propagate into the material of the test specimen. The propagation is constrained by the upper and lower surfaces of the specimen, hence the term guided wave. These interact with features such as defects and reflect back to the same transducer that captures the echo signal [2].

To date, the most common application of LRUT is in the in-situ inspection of industrial pipelines [1], [2]. The effectiveness and the economic viability of the LRUT method led industry to broaden its applications to include condition monitoring of large remote structures or those with limited access for maintenance such as offshore wind-farm turbine towers, tanks and floating production storage and off-loading vessels (FPSOs). These applications require remotely installed, distributed-sensor networks based on the LRUT technique.

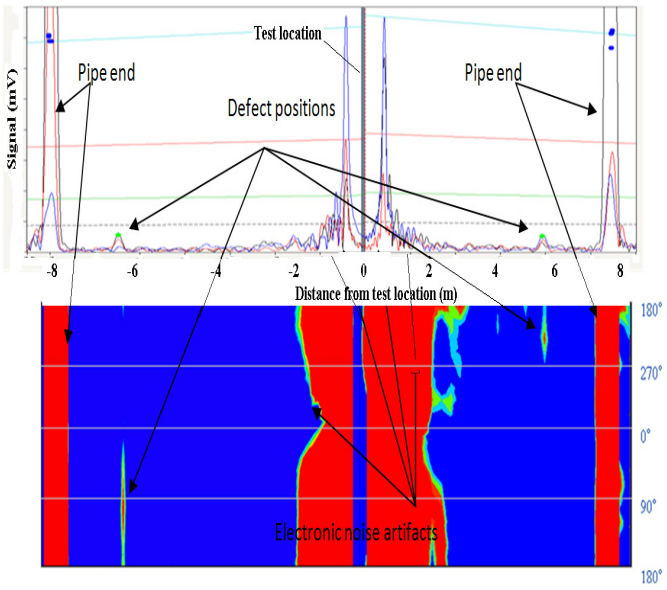

Figure 1. A-Scan and A-Map of the LRUT Applied Pipe [2]

A pulser receiver unit (PRU) allows the LRUT technique to be implemented in remote locations. It is an electronic instrument powered by rechargeable lithium ion (Li-Ion) batteries. Uninterrupted structural monitoring relies on reliable instrumentation. There is evidence that premature failure of remote sensing instrumentation is mainly caused by inadequate power sources [3], [4]. Reliably estimating the power budget of the system is, therefore, crucial for allocating adequate power sources for LRUT instrumentation.

Power consumption can vary for different functions and scenarios. Power analysis on LRUT hardware for various scenarios and functionalities can enable one to specify an adequate power source for the instrumentation that would last for the scheduled inspection period. However, practical experimentation using hardware is not always possible at early stages of the project, nor is it feasible to run such experiments for all scenarios. Computer system modeling of the LRUT system forms a virtual test platform that can be used for power analysis and optimization without the need for any hardware.

System Modeling Concept

Accurately modeling the inter-coupling nature between different engineering disciplines and simultaneously simulating the constructs on a single platform is crucial for understanding the system. There are high-end tools such as Saber and System-Vision from Cadence and Mentor graphics, respectively, which allow multi-engineering discipline systems to be modeled and simulated on a single platform, but they require specialized knowledge in all relevant engineering disciplines. The cost of licensing these tools is also high and disproportionate to most project costs. Computing power requirement is also intense.

SPICE is a computer modeling language, which allows equivalent circuit models of different engineering disciplines to be modeled in the electronic domain. LTSpice is a free SPICE-based simulation tool developed by power product company Linear-Technology. It allows models to be inputted with their relevant parameters and simulated simultaneously on a single simulation platform. This method requires minimal knowledge of other secondary engineering disciplines, and simulation time and computing power are affordable, due to the simplistic algorithms and relaxed parameters.

The LRUT system consists of multi-engineering-discipline constructs such as electrochemical (battery model), electromechanical (transducers - load) and analog-digital mixed-signal electrical components. SPICE-language -based equivalent circuit models have been developed for simulating foreign domain constructs in SPICE-based simulation tools [5], [6]. However, there is a trade off in the accuracy of equivalent circuit model simulation results compared with the real system. Topology-specific models have been used in modeling work for power and functionally sensitive constructs. Presented here is the modeling and related practical work carried out on the load, transmit-circuit and the high-voltage power supply in the associated system that has significant influence on power performance.

The LRUT System Model

The simplified version of the LRUT system model using LTSpice is shown in Figure 2. It includes several constructs such as transmit circuit, transmit/receive transducer array (PZT_Array), test specimen (Pipeline) and receive circuit (Preamp). The system model represents a pulse-echo mode of operation. The pipeline was modeled using a lossy transmission line model. It has an integrated feature (e.g. defect-weld – acoustic impedance mismatch) and the pipe end is terminated at an acoustic impedance equivalent to air. Each transducer in the transducer array is damped with a stainless steel backing block; more details are given in the load characterization section. This LRUT system model not only allows for analysis of the power performance of the system, but also allows port dynamics to be analyzed for signal strength.

Ultrasonic piezoelectric transducers (lead-zirconate-titanate - PZT) are often used as transmit and receive sensors in LRUT techniques. The capacitive nature of these PZTs requires a high-voltage stress (excitation voltage) to force them into oscillation and to achieve a high signal-to-noise ratio. This high excitation voltage signal needs to be short (broadband) in order to achieve better resolution [7-9].

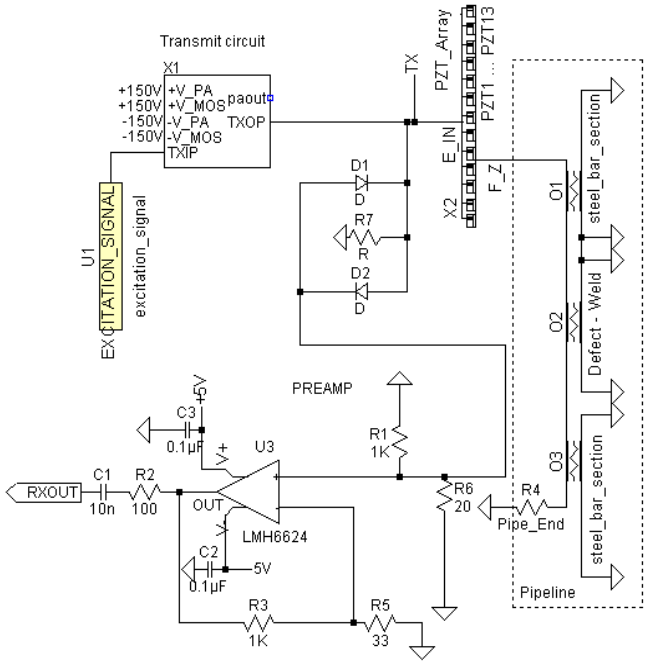

Figure 2. Simplified LRUT System Model Constructed in LTSpice

The LRUT application uses a $240V_{pk\text{-}pk}$ electrical signal in the frequency range of 20kHz to 100kHz. The technique requires a number of excitations (and data collection) at a repetitive rate (rep-rate) of 0.1s for data manipulation. The main circuits involved are the transmit-circuit (TX), receive -circuit (RX), high-voltage power supply (CCPS) and the digital logic control circuits (DSP). The TX circuit produces a high-voltage, high-current electrical signal that excites the transducer array (load) that in turn produces the sound waves. The receive-circuit allows reception and signal processing of the echo signals from features. CCPS is a fast capacitor-charging power supply that produces +/-150V on demand, which provides voltage to the TX. The DSP handles system control, signal processing, storage and communication.

Load characterization

Load charecterisation is required for specifying the PRU's port dynamics and power performance. Load for the PRU is an array of PZT transducers of the type EBL#2 [10] that are pre-engineererd with damping blocks and faceplates. A number of equivalent circuit models for PZT transducers are discussed in the literatue [5]. This work employed a single-dimensional-thickness mode Krimholtz, Leedom and Matthaei (KLM) model, as the KLM model allows additional layers such as face plates and matching layers to be easily added on to the model. Faceplates and matching layers can be modelled using the lossy transmission-line model. The derivation of parameters used in the KLM model for the PZT transducer requires three basic parameters that can only be obtained using practical measurements or by using equations [11]. They are free capacitance (C^T), resonant frequency (f_p) and anti-resonant frequency (f_a) of the transducer. A Solartron SI1260 impedance analyzer was used for the practical impedance analysis. The measured free capacitance was approximately 1100pF at an excitation frequency of 1kHz. The resonant frequency (f_p) and anti-resonant frequency (f_a) were measured as 1.7MHz and 2.4MHz, respectively. Another study claimed that for transducers having a thickness very much smaller than the other dimensions, the vibrations in directions other than thickness are insignificant for modeling purposes [12]. Hence, this single-dimensional model is adequate for the modeling process considered here.

Practical input-impedance analysis results were compared with the simulation results across the frequency range of interest. Figure 3 compares the simulation and practical results obtained for a single PZT. Impedance and phase graphs are set to show 20% and 2% error bars, respectively. A good agreement within 20% was obtained between the simulation and practical results.

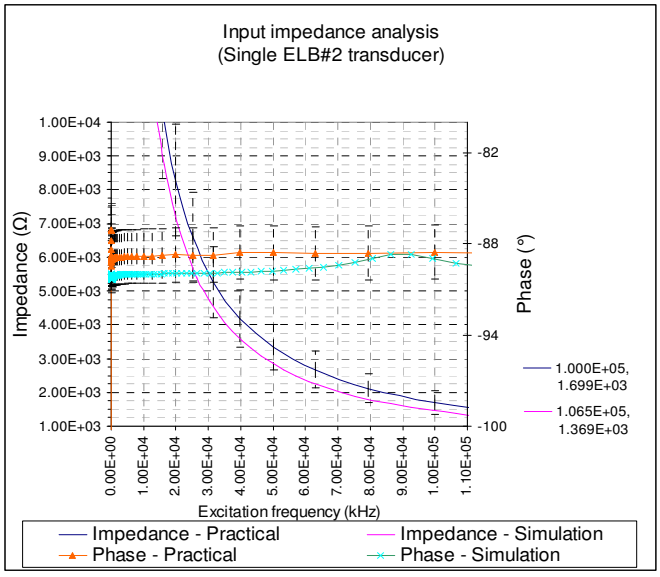

Figure 3. Input Impedance Analysis of a Single Domain PZT

In LRUT applications, PZT elements are mounted to stainless steel backing blocks for damping and mounting purposes. This transducer fabrication also includes a faceplate for acoustic impedance matching and durability. The PZT transducer with backing block and faceplate is called an LRUT transducer. Each output port in the PRU system is specified to drive an array of LRUT transducers. The array size can be as big as 13 LRUT transducers connected in parallel.

The total input impedance analysis for an array of 13 LRUT transducers was also carried out practically and through computer simulations. Faceplates were modeled using a transmission-line model. The stainless steel dampers were modeled with resisters, whose values were calculated using the acoustic impedance formula, $R = \rho A u_p$, where ρ, A and u_p were the density of stainless steel, cross sectional area and phase velocity, respectively [13]. The practical and simulated results are shown in Figure 4. Discrepancies within 30% were observed between practical and simulation results. As the operating region of the LRUT application was well below the series resonance frequency of the PZTs, the load held capacitive properties as expected [11]. This can be seen in Figure 3, where the phase angles are around negative 90 degrees (-90°).

A maximum of 40% variation in input capacitance was observed when practical tests were carried out on two batches of 77 transducers (within and between the batches). Hence, the 30% discrepancy observed in Figure 4 was acceptable. It was concluded from the modeling work that the minimum value of load impedance was 115Ω±30% (80.5Ω), which was confirmed through practical results.

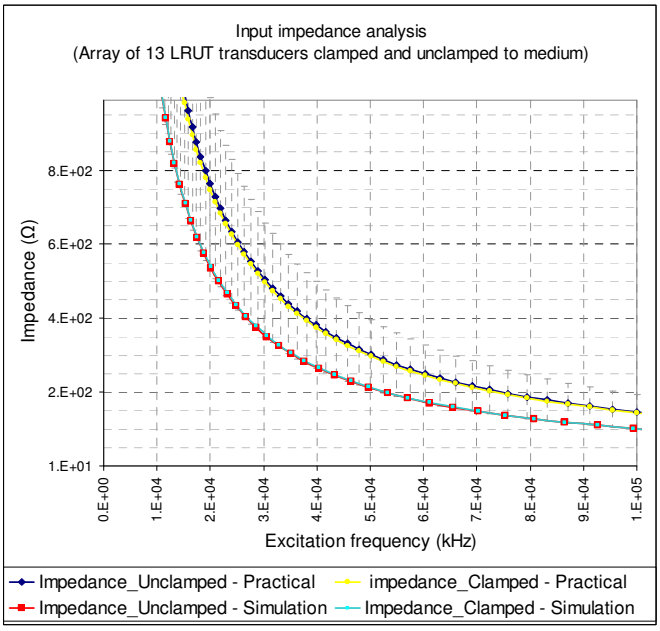

Figure 4. Input Impedance Analysis of an Array of 13 PZT

Transmit Circuit

A transmit circuit capable of exciting a capacitive load with an equivalent impedance of 80.5Ω (70% of the 115Ω for the minimum stated above) was modeled, simulated and prototyped. Using the TX circuit specifications shown in Table 1, design constraints such as slew rate, peak load current and the instantaneous power consumption of the circuit were calculated as 75.3V/µs, 1.5A and 178W, respectively [14], [15].

Table 1. Transmit Circuit Specification

Parameter	Symbol	Range
Tx Supply Voltage	+Vs and -Vs	±150Vdc
Excitation signal frequency	F_{exc}	20kHz-100kHz
Load Value	Z_{total}	115Ω±30%
Excitation Voltage	V_{exc}	±120Vpk
Input signal	Vin	1Vpk-pk
Inverting fixed gain	G	150(43dB)
Number of sine waves per transmit envelop	N_{cycle}	Max 20 Min 10

A complementary MOSFET arrangement, as shown in Figure 5, can provide the required high slew rate, high-voltage excitation waveform and load current demand. The circuit arrangement consists of a single, high-voltage power amplifier (PA) and high-voltage N-type and P-type metal-oxide semiconductor field-effect transistors (MOSFET). The complementary MOSFET arrangement acts as a current source and provides the required load current that the high-voltage PA cannot provide alone. Steele and Eddlemon [16] provide a detailed operation of the circuit. Resistor R_{gs} was chosen to guarantee the maximum required V_{gs} (obtained from MOSFETs datasheets) for the MOSFETs with the PA output current limit [15]. The added auxiliary circuits provide circuit and load protection. The combination of U2-Q1-Rcl+ and U3-Q2-Rcl- provides the current limit protection in the event that the load current exceeds the maximum load current of 1.5A. R6 is a high-value resistor, which provides additional protection for the PA (limits the PA output current), should the MOSFETs open. D1 and D2 are zener diodes that limit the V_{gs} to the maximum specified V_{gs}.

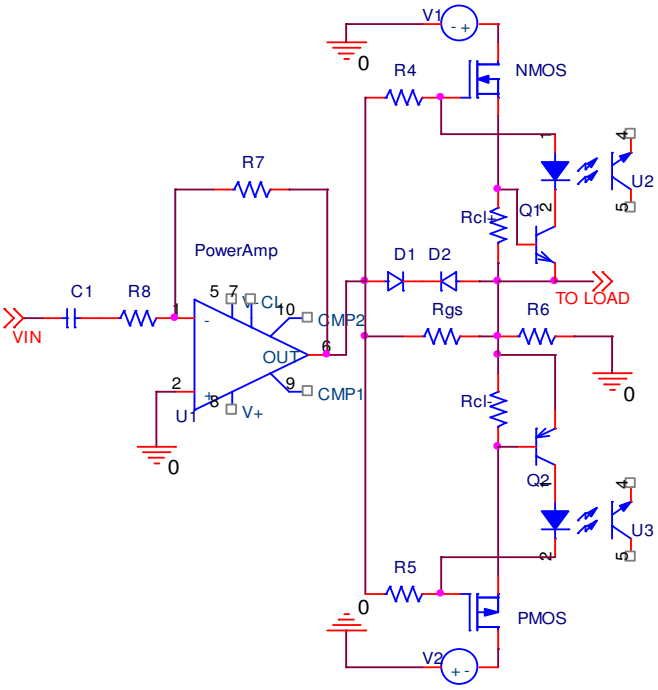

Figure 5. Transmit Circuit

A number of simulations were carried out on this circuit to evaluate stability, SR and, most importantly, power consumption and dissipation at the component level. Simulation results showed that approximately 10% of the supply voltage drops across the MOSFETs and the PA during excitation, generating heat, thus requiring heat sinks. Figure 6 shows the power performance of the circuit for the heaviest load (80.5Ω). It can be seen that the peak instantaneous power consumption of the transmit circuit is about 200W at the excitation frequency of 100kHz for the aforementioned

load characteristics. High current and voltage spikes at the rising edge of the waveforms are due to the short-circuit behavior of the capacitive load at the initial stage (before charging). The quiescent current of the PA was about 10mA [15]; for the applied potential of $300V_{pk\text{-}pk}$, the quiescent power consumption of the circuit was about 3W. This is also noticeable in Figure 6. The simulation results for power consumption were higher than the calculated value (177W) as the calculation steps did not account for power consumption and losses in the auxiliary components. The results presented in Figure 6 also show that the load current was 1.5A at a frequency of 100kHz.

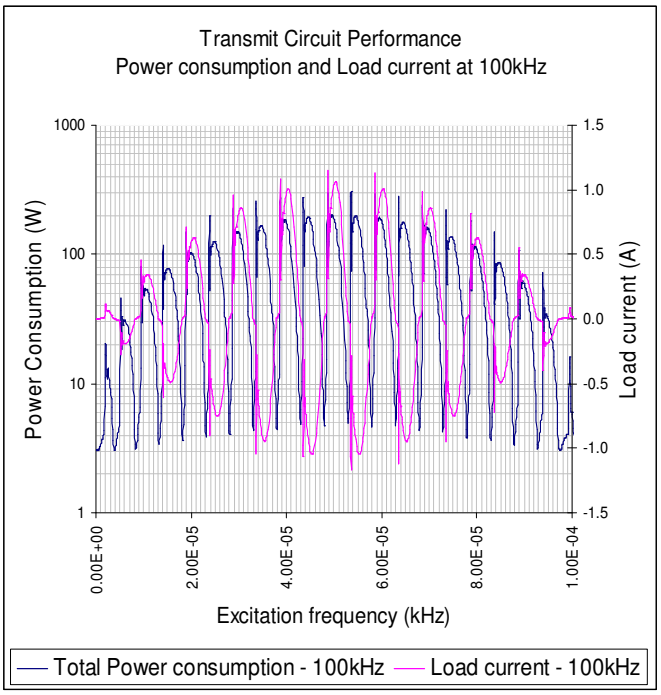

Figure 6. Transmit Circuit Performance

The transmit envelope maximum duration was calculated as 1ms using Equation (1), the values for which are given in Table 1.

$$TX_{duration} = N_{cycle} / F_{exc\_min} \qquad (1)$$

The implication of Equation (1) is that the energy utilized by the transmit circuit per transmit cycle is 200mJ (200W x 1ms). A typical PRU can support 24 of these loads, hence 24x 200mJ is consumed immediately. A steady power supply is, therefore, required to provide 200mJ, while maintaining the power rails at +/-150V (low ripple) for each transmit cycle.

High Voltage Power Supply

Normally, power to this type of pulsed load is provided using bulk capacitor banks. In this scenario, energy is stored in capacitors and discharged to the load upon demand. Topping off the capacitor bank is required in order to maintain the voltage between repetitive load pulses. A typical PRU requires separate capacitor banks for +150V and -150V rails with 1,600µF, totaling 3,200µF.

Push-pull converter topology and flyback topology are commonly used in rapid capacitor-charging processes. Push-pull topology is generally used in applications where power requirements are above 200W. A flyback topology was selected for this application due to its simplicity, size, low cost and its widespread use in power applications requiring power levels below 200W [17]. A single-stage flyback CCPS was modeled for meeting the specification of charging a 2x1600 µF capacitor bank within 2s of initial demand and keeping the +/-150 V supply regulation within 4% of target.

The operation of flyback power supply is explained in a report by Basso [17]. The only difference between that work and this study is the split power-supply design. This was achieved using a center-tap transformer. Figure 7 depicts the simplified schematic diagram of the dual–rail, single-stage flyback converter circuit. In flyback topology, transformer T1 is used for maximum energy storage purposes. Hence, it is built with air gaps in the core to trap the energy in them.

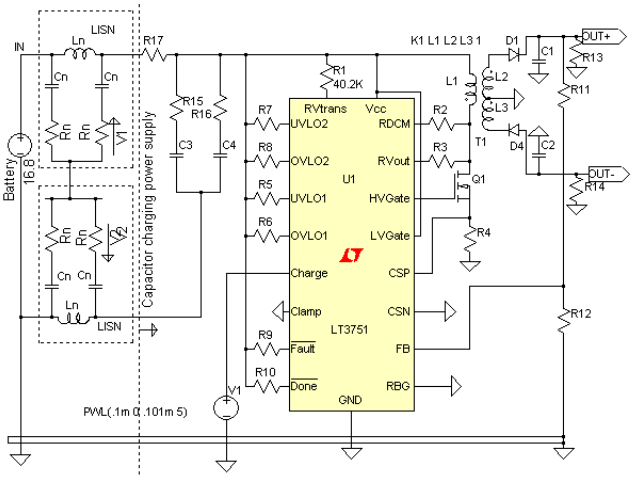

Figure 7. CCPS based on Flyback Topology

When switch Q1 is turned on, the current in the primary inductor (L_1) ramps up with the flux storing magnetic energy. A voltage is induced across the secondary winding (L2, L3) of a polarity such that D1 and D4 are reverse-biased. Hence, no current flows in the secondary circuit. When Q1 is turned off, the primary current drops to zero and the voltage across secondary windings L1 and L2 reverses, allowing D1 and D4 to conduct current that, in turn, charges capacitor banks C1 and C2.

Flyback topology can be used in either discontinuous current mode (DCM) or continuous current mode (CCM). In general, low–voltage, high-current applications use CCM and high-voltage applications use DCM. As this is a high-voltage circuit (transmit current is only drawn from the capacitor banks), DCM is appropriate, but this method is less efficient and tends to heat up the magnetics and the switching device [17]. Boundary mode (BM) operation is also appropriate for this application. In BM, the switching current drops to zero as soon as the switch opens, which make the CCPS very efficient.

There are a number of components which need to be selected before carrying out topology-specific modeling and simulation of this CCPS. They were calculated and listed in Table 2 [18]. A correct selection is important in order to achieve the specified performance.

Table 2. Component Rating for CCPS

Component	Constrains
Transformer inductor	Primary Inductance 11μH; turns ratio 1:10
Switching device N-Type MOSFET	V_{BR} > 32V; $I_{d\text{-}average}$ > 0.94A
Output diodes – Rectifiers	V_{RRM} = 320V or better; $I_{F(AV)}$ > 200mA
Peak Primary current (I_{PRI})	4A

The power-source protection circuits in the PRU are specified to handle the maximum of 10A. The PRU has other circuits that require considerable amounts of current while the capacitor bank is charging. Hence, the primary peak current (I_{PRI}) that the CCPS would use during initial charge up was limited to 4A using R4 in Figure 7.

Simulation results that demonstrate the model fitness of the CCPS are presented in this section. Figure 8 shows the V_{ds} (drain-source voltage) across the switching device, Q1, where I_d is the drain current switching through Q1 when Q1 is turned on. It is clear that the drain of the MOSFET is experiencing an approximate 60V spike due to stray inductance and high di/dt at turn off. The selected MOSFET was rated at 150V, 5A (pulsed current). The drain current, I_d , passing through Q1 when switched on was limited to 4A in the calculation, though the simulation showed that I_d could reach a peak value of 4.2A.

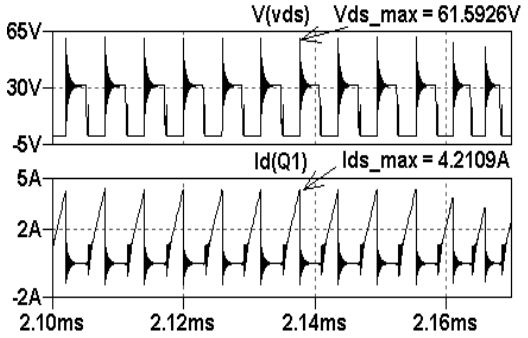

Figure 8. Simulated Switching Device Performance

Figure 9 shows the current passing through the output diode (D1). Average and peak diode current values of 64mA and 240mA were observed. This was expected as calculations indicated that the peak diode current is approximately I_{PK}/2N, or 200mA. The diodes selected for this application can handle 1A peak current. A fast Fourier transform (FFT) of the Q1 switching signal was also probed during simulation to find the maximum switching frequency.

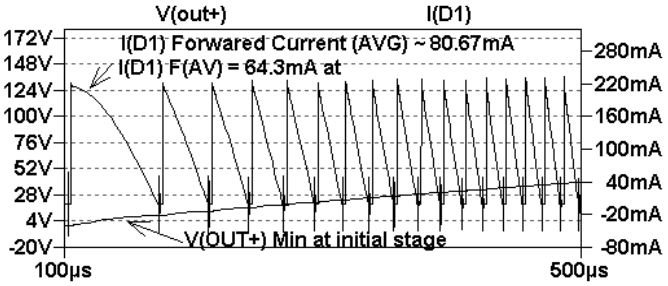

Figure 9. Simulated Rectifier Diode Current

The results are presented in Figure 10 and show Q1 as being switched on at a maximum switching frequency of 150kHz. This value was also used to specify the flyback transformer. For a 20W design, the switching frequency can be between 100kHz and 200kHz [18].

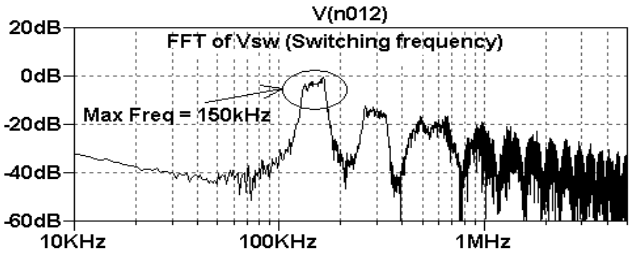

Figure 10. FFT of Switching Signal: Q1 Gate Drive Signal

The amount of electromagnetic interference (EMI) this switch-mode power-supply circuit introduces to the PRU can affect the ultrasonic performance of the system. It is necessary, then, that any EMI within the frequency spectrum from 20kHz to 100kHz would need to be kept below a noise value of -72dB. Differential-mode (DM) and common -mode (CM) noise were evaluated in the simulation using a line impedance stabilization network (LISN) at the input and output (not shown). Differential-mode noise is generally generated due to high di/dt (fast switching) effects on stray inductance. Common-mode noise is generally due to dv/dt effects. This can propagate through the PCB tracks. Localized filtering and careful PCB layout are necessary for noise suppression. Figure 11 depicts the FFT of DM (green trace, top) and CM (blue trace, bottom) noise level at the LISNs inserted at the input stage. Similar work was carried out on the output stage as well (before the capacitor bank). Appropriate filtering was included to prevent EMI spreading to sensitive TX and RX circuits.

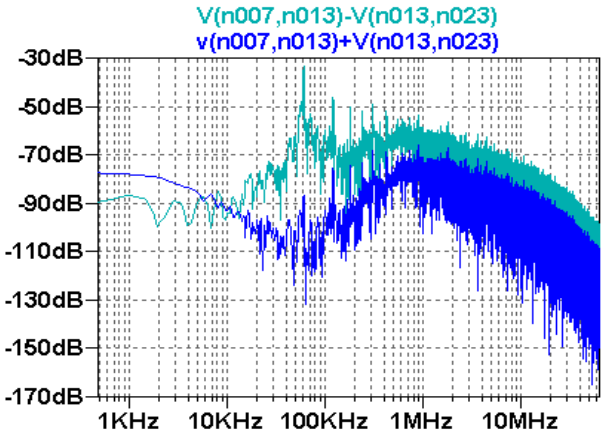

Figure 11. FFT of Differential and Common Mode Noise

Figure 12 highlights the BM-mode operation of the efficient flyback topology. As can be seen, the drain current of Q1 (I_d) drops to zero with the Q1 switching signal (V (n012)), i.e., in BM the primary inductor current (I_{PRI}) drops to zero as soon as the switch (Q1) opens, allowing efficient transfer of energy. The efficiency of the CCPS circuit was analyzed through simulation for varying input voltages (battery voltage) from 13V to 16.8V in 1V steps. Consistent efficiency of 87% was observed for both light and heavy loads.

Practical Validation

Practical results for evaluating the load model were discussed in the load-characterization section. A prototype of the modeled CCPS was produced and practical tests were carried out. Some experimental results are presented to show the validity of the model developed here.

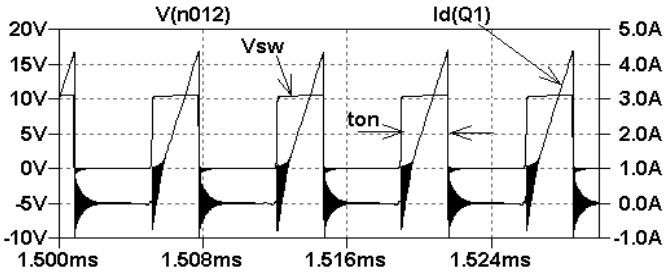

Figure 12. Simulated Boundary Mode Operation of CCPS

Figure 13 depicts the practical measurement taken on the prototyped CCPS for Q1, drain current I_d (CH1/R4), output voltages +150V (CH3), -150V (CH4) and the switching signal (CH2). I_d was measured as high as 18A initially and then dropped to 4A during charging as set by R4 in Figure 7. The initial 18A surge was of short duration and can be tolerated by Q1. In simulation, initial I_d values were seen as high as 26A (not shown in this paper). Maximum switching frequency was measured as high as 179kHz, as shown in Figure 14.

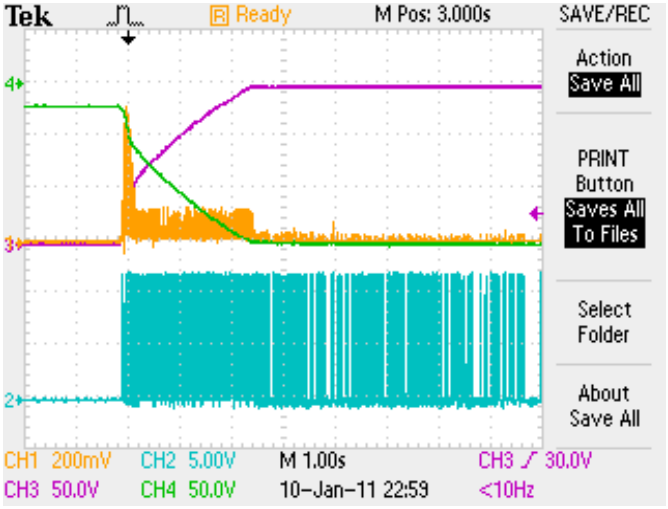

Figure 13. Performance of CCPS - Measured

The voltage stress that the switching device, Q1, experienced (V_{ds}) during switching off and the mode of operation of the CCPS were probed and are portrayed in Figure 15. As can be seen (CH4), the drain voltage, V_{ds}, peaks at 60V when Q1 switches off. The simulation results depicted in Figure 8 also predicted similar values for V_{ds}. The choice of a 150V breakdown voltage for the MOSFET (Q1) was because it could handle this voltage stress. The need for a snubber circuit and the unnecessary power dissipation in the snubber resistor can be avoided by carefully selecting the

device and keeping the PCB tracks short. BM operation is maintained as the drain current of Q1 (CH1) drops down to zero when Q1 is turned off (switching signal - CH2). Other CCPS-related practical results validating the model were obtained, but are not included here.

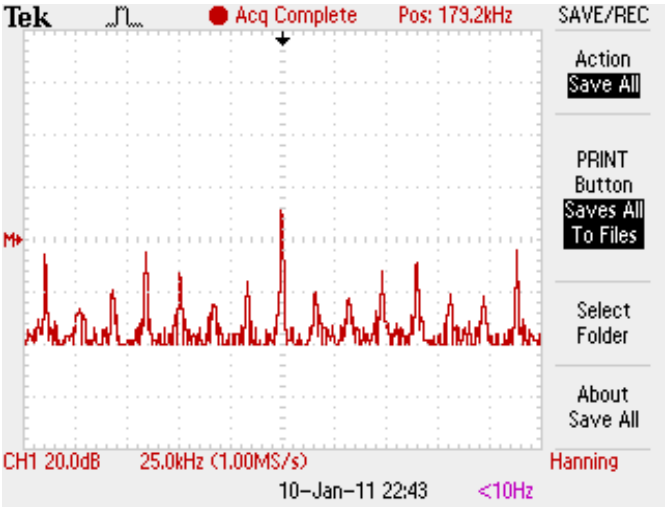

Figure 14. Maximum Switching Frequency of Q1

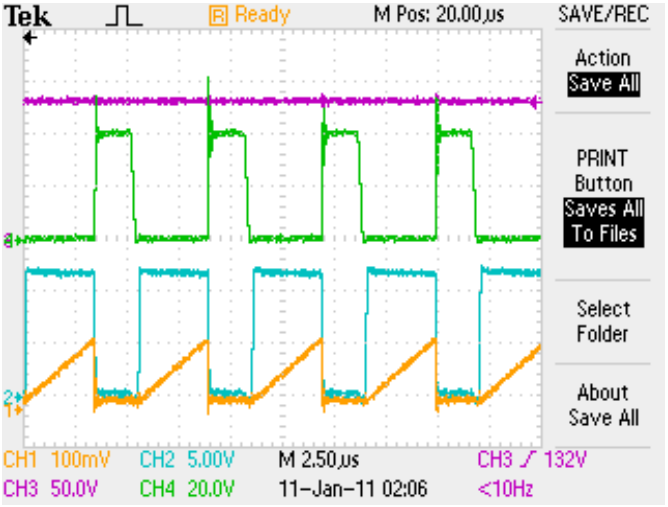

Figure 15. Performance of Q1 and BM Operation

The transmit circuit excitation signal of voltage +/-140V at 50kHz is shown in Figure 16, revealing no cross distortion or slew rate limitation. A voltage drop of 20V across the PA and the MOSFETs of the transmit circuit (Figure 5) was noticed when a +/-150V excitation pulse was demanded at the transmit circuit output, thereby causing voltage clipping at +/-140V.

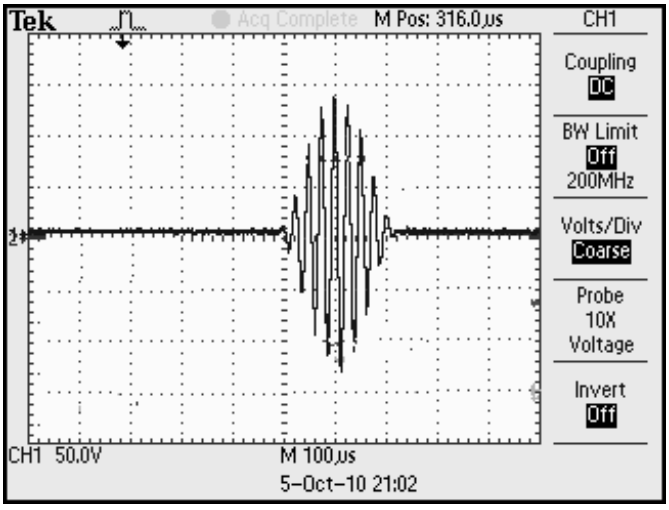

Figure 16. Transmit Circuit Output - Measured

Power Budgeting

A typical power-consumption profile for the modelled LRUT system for one complete inspection cycle (test) was predicted using simulation. A SPICE-based equivalent circuit model of a Li-Ion battery pack was used as a power source for the simulation [6]. The simulation data was used to obtain the adequate power-source capacity value. For both simulation and live measurements, Figure 17 shows how the power source (battery) terminal voltage drops according to the number of tests. The cut-off terminal voltage of a series-connected 4-cell 3.3V (nominal volts) Li-Ion battery pack is about 12V, meaning that the maximum number of complete tests that can be carried out before the likelihood of system failure due to lack of power is 12.

Hardware Realization

A commercial product was manufactured based on the modeling and the prototype and launched at the American Society for Nondestructive Testing (ASNT) spring conference in March 2011 (in Houston, Texas). The production version of the PRU and the model of the internal layout—showing the integrated rechargeable Li-Ion battery—are portrayed in Figures 18(a) and 18(b), respectively. Practical tests carried out on the manufactured PRU revealed that a fully charged power source allowed 20 complete inspection cycles. This satisfied the predicted performance of 12 inspection cycles stated above (an extra 50% battery capacity was added in the production version as a conservative measure to allow an extra 8 inspection cycles for a total of 20).

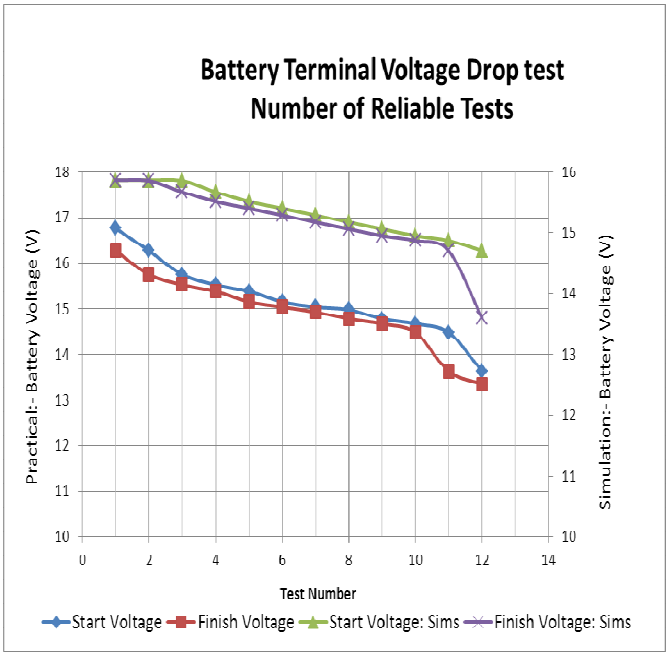

Figure 17. Battery Terminal Voltage versus Number of Tests

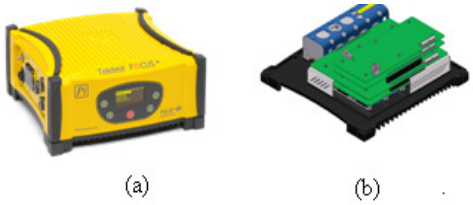

Figure 18. Picture of PRU Product Launched

Discussion

A systematic approach to system modeling allowed rapid prototyping of this industrial application product. It also allowed the developers to avoid over engineering and respinning of the design concept. Close mapping of the simulation results to the hardware results provided a reliable, virtual test platform that industry can use for further enhancement of the product family and foreseeing uncertainties. This research and engineering application work differs from previous work as the system model developed here allows all relevant constructs, regardless of their engineering disciplines, to be integrated and simulated in a single electrical domain simulation platform providing a unique contribution to knowledge.

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