CHARGE CONDUCTION MECHANISM AND MODELING IN HIGH-K DIELECTRIC-BASED MOS CAPACITORS

Madhumita Chowdhury, The University of Toledo; Branden Long, The University of Toledo; Rashmi Jha, The University of Toledo; Vijay Devabhaktuni, The University of Toledo

Abstract

In this study, four MOS capacitors were fabricated (Al_2O_3/Ti, Al_2O_3/W, HfO_2/Ti, and HfO_2/W) on Si substrates. Temperature-dependent measurements were performed to study the gate leakage current. To investigate the metal/high-k dielectric interface, charge transport mechanisms of the gate leakage current were examined. I-V curves were fitted to three main conduction methods, i.e., Frenkel-Poole (F-P) emission, Schottky emission, and tunneling mechanism, at both low and high electric fields with barrier heights extracted. Furthermore, to improve device-to-device uniformity, simplify the process of data acquisition, and increase yield, a neural network was employed to model the I-V relationships across different temperature ranges for all four samples.

Introduction

Gate leakage current is becoming the bottleneck in the design of high-speed and low-power consumption devices due to continuous scaling of the dielectric thickness of SiO_2 [1]. The continuous reduction in the thickness of the gate dielectric (SiO_2) results in very high gate leakage current due to direct tunneling of electrons through the SiO_2. This would finally lead to high power consumption even when the device is off, i.e., the gate voltage is less than the threshold voltage [2]. To ensure that Moore's Law remains valid in the next decade, leading integrated circuit (IC) manufacturers are now making a breakthrough by replacing the long-standing poly-silicon gate and SiO_2 [3] with a metal gate like Ti, W, Pt and high-k dielectrics such as HfO_2, Al_2O_3 and TiO_2 , respectively [4], [5]. The reason for replacement of poly-silicon gates with metal gates is to avoid high threshold voltages which arise due to Fermi-level pinning along with degradation of channel carrier mobility [6-8]. Fermi-level pinning is nothing but an inability to entirely move the Fermi level (E_F) across an Si band gap [9], [10]. Metal-induced gap states (MIGS) generated at poly-Si/SiO_2 interfaces tail off very quickly into the SiO_2 and cause very little pinning, for which E_F can be shifted completely through the Si gap by varying the work function of the electrode. However, in poly-Si/HfO_2 interface MIGS are more in number and die less swiftly when compared with SiO_2. Hence, a larger alteration in work function would be needed to oscillate E_F across the Si band gap [11]. A high-k-based dielectric helps in maintaining the same capacitance as that of a SiO_2 dielectric but with a thinner material layer [12].

However, in order to replace the longstanding combination of poly-Si/SiO_2 material with a metal/high-k dielectric, it is imperative to fully comprehend the interface mechanism. This can be done by studying the mechanism of charge transportation of gate leakage current. In spite of significant research progress in this area, the mechanism of charge transport responsible for the gate leakage current and its dependence on the gate dielectrics and metal electrodes is not well understood. To address this problem, the authors evaluated the charge conduction mechanism of gate leakage current in different high-k-dielectric-based MOS capacitors with metal electrodes on top. In addition, temperature-dependent measurements were made to compare the charge transport mechanism of atomic layer deposited (ALD) HfO_2-based MOS capacitors with that of Al_2O_3-based MOS capacitors with Ti and W electrodes. I-V curves were fitted for different conduction mechanisms at different temperature and voltage ranges. A neural network method of modeling was employed to ease the duplication of the same sample by avoiding calculating parameters like effective mass of an electron and material-specific parameters, which reduce the cost of fabrication and increase the speed of data acquisition.

Background

The reduction of the gate dielectric thickness is one of the core reasons for increases in gate leakage current of MOS devices [13]. To minimize this gate leakage current, many high-k gate dielectrics have been recommended as substitutes for SiO_2 in MOS structures with effective oxide thicknesses (EOT) lower than 1.5nm [14]. To better study the interface, temperature-dependent measurements are among the most important methods for determining the charge transport mechanism of the gate leakage current. A temperature-dependent study was performed on Ta_2O_5 and TiO_2 films to determine their conduction mechanisms and to verify whether the gate leakage current is supportable at high temperatures for either of these high-k dielectrics. From studies it was found that in Ta_2O_5, I–V curves showed stronger temperature dependence than in TiO_2 samples [15],

[16]. The chief reason was a lower electron barrier height in Ta_2O_5, which resulted in Schottky emission to dominate the charge conduction mechanism. On the contrary, the TiO_2 sample demonstrated tunneling as the dominant conduction mechanism in the high-field region, and F-P conduction in the low-field region. In the literature, it was reported that, for an HfO_2 dielectric, a high work function metal (Pt) would be responsible for the F-P emission conduction mechanism [17]. This is because the Schottky barrier height would be larger than the energy level of the traps. However, for an Al electrode, the Schottky emission dominated the conduction mechanism of gate leakage current. On the other hand, it has been proved that Al_2O_3-dielectric-based MOS capacitors with Al electrodes showed the F-P emission to be the dominating charge transport mechanism at the Al/Al_2O_3 interface [18].

In spite of these studies, a rigorous comparison was needed to identify which conduction mechanism dominates at which voltage level and temperature range for a specific metal/dielectric interface. In this study, a temperature-dependent comparison was made at different voltage ranges to identify the dominant current conduction mechanism. In addition, a neural network model based on a Quasi-Newton algorithm was employed for ease of sample reproduction by avoiding extracting parameters like barrier height and effective mass from equations which are labor-intensive and time -consuming processes. Neural network's ability to learn quickly for building convincing solutions to unformulated problems, manage computationally expensive models, deliver fast interpolative analysis, and attain very precise functional relationships between data sets are its major advantages [19]. It is a well-established method for modeling various processes in the semiconductor industry such as molecular beam epitaxy and plasma-enhanced chemical vapor deposition [20]. In a review of the literature, modeling of semiconductor process device characteristics was done in both the forward and inverse directions [21]. A multilayer perceptron neural network (MLPNN) was used for development of the model. In the forward direction, data obtained from the characteristics of earlier fabrication processing points were used as input to a MLPNN, and the last characteristic values were modelled. On the other hand, for inverse modeling, final DC device characteristic measurements of the total wafer were used as input to an MLPNN, and in-process characteristic data were modelled. This method eliminates the necessity to statistically describe parametric deviation across a wafer. In this study, modeling of gate leakage current was implemented for reducing the non-uniformity in the fabrication process and collecting additional data without fabricating the samples again.

Methodology

This section is divided into two parts: the experimental processes and the neural network modeling approach. The first section deals with the fabrication of the MOS capacitors while the latter discusses the modeling method used to calculate the output current.

Fabrication Process

HfO_2 and Al_2O_3 dielectric films were deposited on p-type Si wafers by an Atomic Layer Deposition ALD process at 300°C. The thicknesses for both of the dielectrics were measured to be ~60Å using an ellipsometer. W and Ti metals (gate electrodes) of 1,000Å were deposited by RF sputtering and were patterned by the lift-off technique. The back contact was formed by depositing 1,000Å of Al on the backside of the samples by RF magnetron sputtering followed by rapid thermal annealing (RTA) in an N_2 environment at 600ºC for 5 minutes in order to achieve a low-resistance ohmic contact. The samples were probed in the Lakeshore cryogenic probe station and I-V characteristics were obtained by a Keithley 4200 Semiconductor Characterization System.

Neural Network Modeling

The modeling of the collected data (gate leakage current) was done using a feed-forward neural network, which consisted of an input layer, a hidden layer and an output layer, as shown in Figure 1. Each layer was comprised of several elements called neurons, where the input layer was a relay function, the hidden layer was a sigmoid function and the output layer was a linear function of hidden neurons. Each neuron in a layer had an input from a previous layer and a constant (or bias), while its output was forwarded to the next layer. The inputs and outputs of the neuron were multiplied by a factor called weights. This feed-forward neural network developed a model from the training data supplied. The network is said to be feed forward because each component/element in a layer receives inputs only from the components/elements in the previous layer. In this study, the modeling was done by covering the entire range of temperature points between 300K – 400K using a Quasi-Newton algorithm. First, the data set available from the experiment was randomized and then segregated into two sections, namely a training data set and a validation data set. Voltages (-4V to 4V) and temperatures (300K, 350K, 400K) were taken as the two inputs for the neural network and current (corresponding to the voltage range) as the output. Out of all the data points, 80% were taken to train the neural network and 20% for validating the results. The neural net-

work approach was taken for modeling because the same or additional results can be obtained again without revisiting the entire process of fabrication and testing. This model will increase uniformity in fabrication, simplify the data acquisition process and, hence, increase future yield.

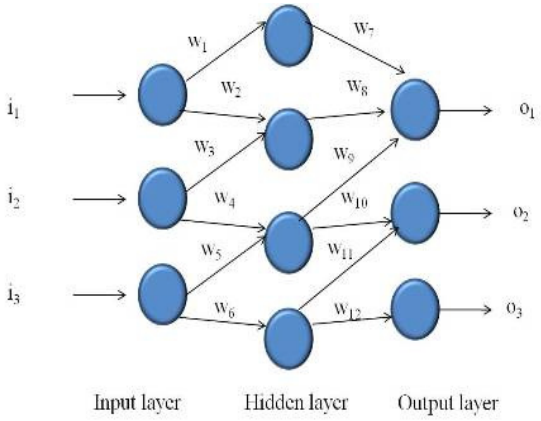

Figure 1. Neural Network Model

Results and Discussions

The room temperature measurements of gate leakage current for all four samples are shown in Figure 2. Currents for both devices with Ti electrodes resulted in much lower currents than those with W electrodes. To further understand their mechanism, temperature-dependent studies of gate leakage current were performed. Gate leakage currents were measured for temperatures varying from 120K to 400K (Figure 3), with an applied voltage of -4V. It was observed that at temperatures below 250K, current was almost constant. Hence, the tunneling mechanism dominates as the primary conduction mechanism for all devices in that temperature range (Figure 3). Above room temperature, any of the three methods—F-P, Schottky emission or tunneling mechanism—may dominate for the samples, depending upon the voltage range [22], [23]. Also, these processes may not be completely independent of each other. It can be seen from Figure 3 that at higher temperatures W-based samples show much-elevated current compared with those of Ti-based samples. For samples using W electrodes, it was observed that more than one mechanism was dominating at the same time. However, for samples with Ti electrodes, the tunneling mechanism was dominant at low temperatures.

I-V curves for all four samples were fitted at 300K, 350K, and 400K employing the following equations:

F-P Emission:

$$J \propto E \exp(-q(\phi_b - \sqrt{(qE/\pi\xi)}/KT) \qquad (1)$$

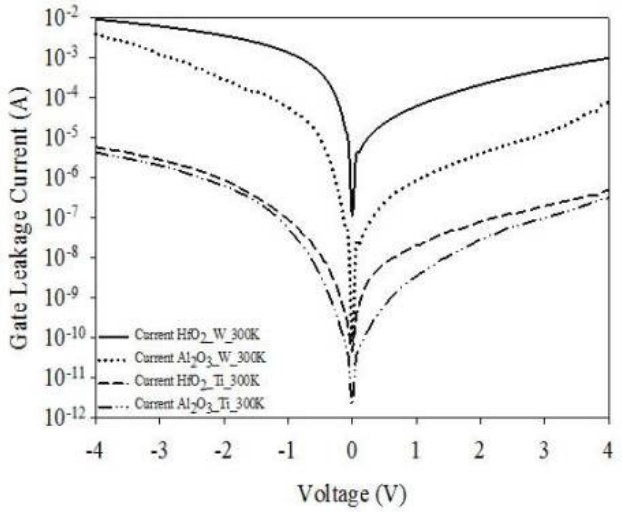

Figure 2. I-V Measurements for Four Samples at Room Temperature

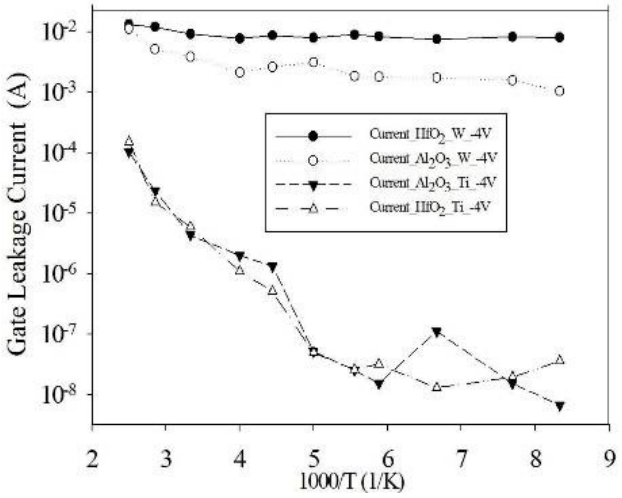

Figure 3. Gate Leakage Current vs Temperature for all Samples

where J is current density, E is the electric field of the insulator, Φ_b is barrier height and ξ is dielectric permittivity.

Schottky Emission:

$$J = AT^2 \exp(-q(\phi_b - \sqrt{(qE/\pi\xi)}/KT) \qquad (2)$$

where A is the effective Richardson constant.

Tunneling:

$$J \propto E^2 \exp(-(4\sqrt{2m}(q\phi_b)^{3/2})/3qhE)) \qquad (3)$$

where m is effective mass.

Observations were split into two cases for data above room temperature (300K, 350K, 400K), depending on the applied voltages. Case 1 dealt with samples in the high field region (-1.5V to -4V) while Case 2 dealt with the samples in the low field region (-0.005V to -1.5V).

Case 1

In the high field region, the I-V curve for sample 1 (Al_2O_3/Ti) fit the Schottky emission model with a barrier height of 0.59eV (Figure 4), while for sample 2 (Al_2O_3/W), the F-P emission dominated. This is logical since for W, the barrier becomes too large for the Schottky emission to dominate. A barrier height of 0.356eV was extracted from the curve fitting, as shown in Figure 5.

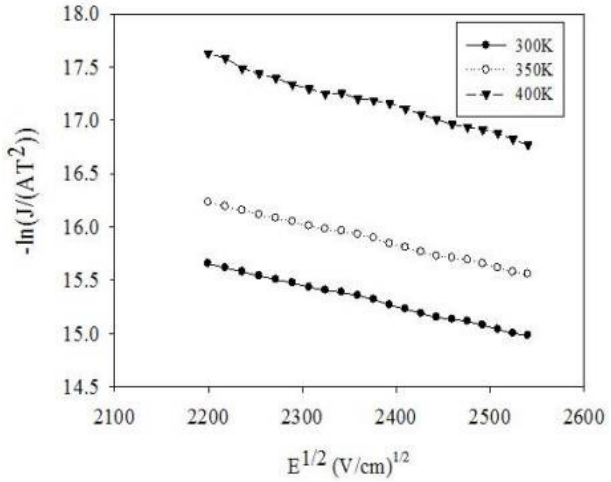

Figure 4. Schottky Emission Curve Fit for the Al_2O_3/Ti Samples at High Field

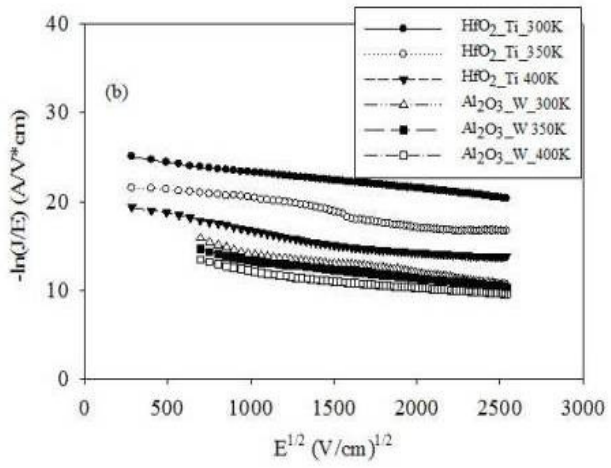

Figure 5. F-P Emission Curve Fitting for Al_2O_3/W and HfO_2/Ti at Low and High Fields

For sample 3 (HfO_2/Ti), the F-P conduction mode fit extremely well, as shown in Figure 6. The calculated Schottky barrier turned out to be greater than the extracted F-P barrier height of 0.58eV. Therefore, at high electric fields, the F-P emission seems to dominate the conduction mode. From Figure 3, it can be interpreted that the current for sample 4 (HfO_2/W) is almost constant, but high relative to samples 1 and 3. The reason could be that, in high electric fields, the I-V curve fits well both in tunneling [24] and F-P conduction mechanisms. Again, it is interesting to note from Figure 7 that the curves are not perfectly overlapping for the tunneling mechanism. This is due to the fact that the charge conduction mode is not independent. Barrier heights of 0.24eV and 0.27eV were extracted for tunneling and F-P emissions, respectively. **A s**ummary of case 1 is depicted in Table 1.

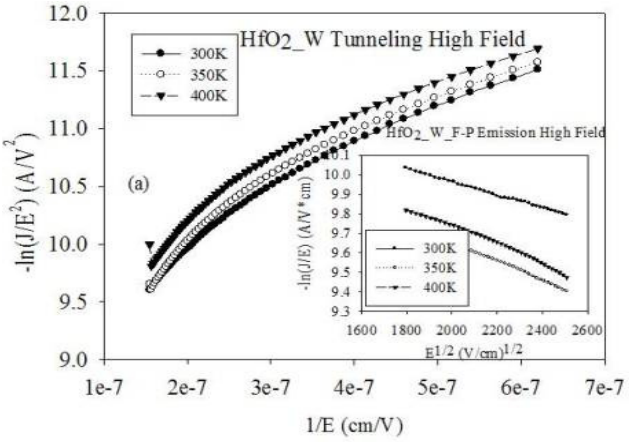

Figure 6. Curve Fitting for F-P Emission and Tunneling for HfO_2/W at High Field

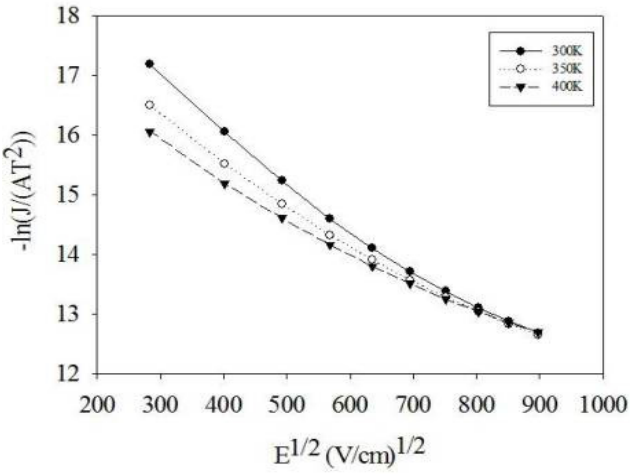

Figure 7. Schottky Emission for HfO_2/W at Low Field

Table 1. Charge Transport Mechanism and Extracted Barrier Heights of Case 1 Samples

Sample No.	*MOS Capacitors*	*High Field (-1.5V to-4V) (Case 1)*	*Barrier Height*
1	Al_2O_3/Ti	Schottky	0.59 eV
2	Al_2O_3/W	F-P	0.356 eV
3	HfO_2/Ti	F-P	0.58 eV
4	HfO_2/W	Tunneling/F-P	0.24 eV/ 0.27 eV

Case 2

In low a electric field, for sample 1, the extracted barrier height of 0.53eV for the F-P emission was less than that of the Schottky emission barrier height, as shown in Figure 8. Therefore, the F-P emission dominates in a low field for sample 1. For samples 2 and 3, the calculated Schottky barrier turned out to be greater than the extracted F-P barrier height of 0.58eV. Hence, the F-P emission dominates in a low field region, as can be seen in Figure 5. However, for sample 4, the Schottky emission acts as the dominant charge conducting mode. A barrier height of 0.49eV was extracted from the curve fitting, as shown in Figure 7. Case 2 is summarized in Table 2.

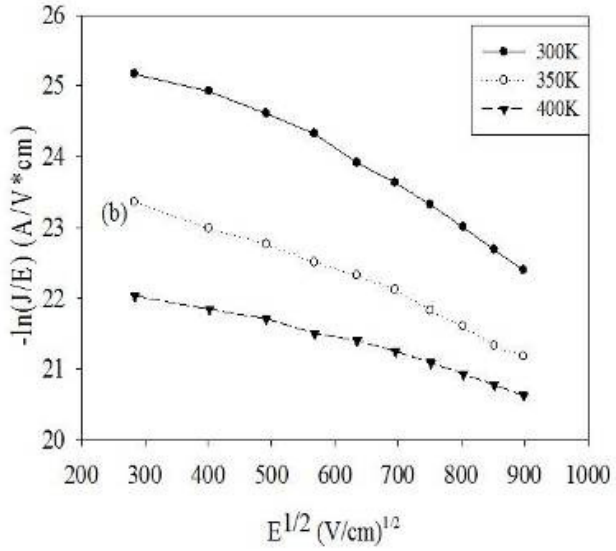

Figure 8. F-P Emission Curve Fit for the Al_2O_3/Ti Sample at Low Field

Thereafter, the modeling of the data was done for all four samples using a neural network to cover all temperature points lying in the range of 300K – 400K for voltage ranging from -4V to 4V, as previously explained in the methodology section. Figure 9 shows the actual output current and neural model output current for all the samples. It can be easily seen that the model followed the experimental set of data very closely. Table 3 shows the training error in the process of modeling the data and validation error after testing the trained model.

Table 2. Charge Transport Mechanism and Extracted Barrier Heights of Case 2 Samples

Sample No.	*MOS Capacitors*	*Low Field (Case 2) (-0.005V to-1.5V)*	*Barrier Height*
1	Al_2O_3/Ti	F-P	0.53 eV
2	Al_2O_3/W	F-P	0.356 eV
3	HfO_2/Ti	F-P	0.58 eV
4	HfO_2/W	Schottky	0.49 eV

Both Figure 9 and Table 3 demonstrate excellent modeling capabilities due to a very low percentage of error. Once modeling is done, the current can be accurately calculated using this model for any given temperature range, which will be beneficial in reproducing the results without actually fabricating the device again. Hence, the model is cost effective and helps in speeding up the entire process of fabrication and testing of devices. On the other hand, the already established equations for F-P emission, tunneling etc. require the definition of a number of parameters like effective mass and barrier height, before calculating the output current. In this way, just by feeding the trained neural network with two inputs (voltage and temperature), the required output (current) can be easily established. In the future, this model would also help in the comparison of different high-k or different metal-gate-based MOS capacitors as reproducing data will be very easy.

Table 3. Training and Validating Errors Obtained from Data Modeling using Neural Network

Error	*Sample 1 (Al_2O_3/Ti)*	*Sample 2 (Al_2O_3/W)*	*Sample3 (HfO_2/Ti)*	*Sample 4 (HfO_2/W)*
Training Error	0.2309%	0.3456%	0.2104%	0.5549%
Validation Error	0.1661%	0.3045%	0.2155%	0.4671%

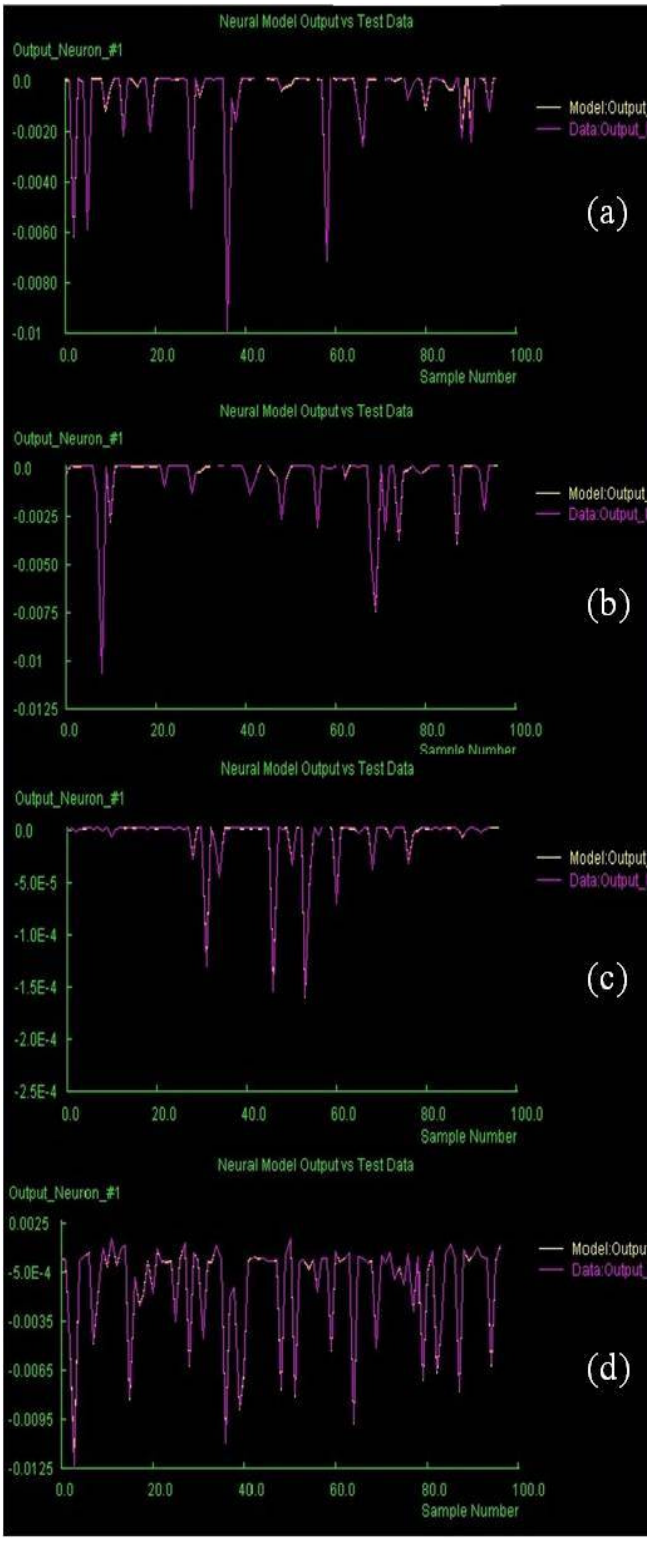

Figure 9. Sample 1 (a), Sample 2 (b), Sample 3 (c) and Sample 4 (d) Shows the Comparison of Actual and Modeled Output Current

Conclusions

The mode of conduction for the four samples consisted of a combination of F-P emission, Schottky emission and tunneling, with each mechanism dominating according to the applied bias and temperature. At low temperatures, tunneling remains as the dominant mode of conduction. However, at higher temperatures and in low field, the F-P emission is the dominant mode of conduction, except for the HfO_2/W sample. In high field, the conduction mechanism is dependent both on the electrodes and dielectrics being used. The neural-network-based modeling of the data proved to be beneficial for predicting the output (current) for different temperature points in the range being modeled without actually fabricating and testing the device. This greatly reduces the probability of manual errors due to fabrication, thereby simplifying data acquisition and improving the yield.

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Biographies

MADHUMITA CHOWDHURY is pursuing her M.S. degree in EECS department at the University of Toledo. Her research interests are fabrication and characterization of resistive RAMS (memristors), compound semiconductors and high-k material-based devices. She is also interested in fabrication of flexible/eco-friendly materials like Graphene to be used as electrodes. Madhumita Chowdhury can be reached at madhumita.chowdhury@rockets.utoledo.edu

BRANDEN LONG obtained Bachelor of Science in Electrical Engineering from the University of Michigan, in 2007, and M.S. in Electrical Engineering at the University of Toledo in 2009. He is currently working towards his Ph.D. degree in the EECS Department at the University of Toledo. His research interests include fabrication and characterization of advanced memory and logic devices, compound semiconductors, thin film transistors, and exploring novel switching mechanisms in semiconductor devices for beyond CMOS applications. Branden Long can be reached at branden.long@rockets.utoledo.edu

RASHMI JHA is an assistant professor in the department of Electrical Engineering and Computer Science. Her research expertise lies in the areas of high permittivity (high-k) transition metal oxide and metal gate electrodes based advanced Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS FET) fabrication and characterization for the next-generation analog, digital, and memory applications. Dr. Jha can be reached at Rashmi.jha@utoledo.edu

VIJAY DEVABHAKTUNI (S'97, M'03, and SM'09) is an Associate Professor in the Electrical Engineering and Computer Science Department, University of Toledo, Toledo, Ohio, USA. He received the B.Eng. degree in electrical and electronics engineering and the M.Sc. degree in physics both from the Birla Institute of Technology and Science, Pilani, Rajasthan, India, in 1996, and the Ph.D. degree in electronics from the Carleton University, Ottawa, Ontario, Canada, in 2003. His research interests include computer aided design (CAD), image/signal processing, modeling, RF/microwave design, optimization and wireless sensing. He can be reached at Vijay.Devabhaktuni@utoledo.edu