PERFORMANCE EVALUATION OF A VARIABLE-SPEED INDUCTION MOTOR DRIVE SYSTEM WITH ACTIVE INPUT POWER FACTOR CORRECTION CIRCUIT

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Abstract

By employing an active input power factor correction (IPFC) circuit as a front-end converter for a variable-speed induction motor drive system, the author was able to demonstrate improvement of the system's power quality, which involved a high power factor (PF) and low total harmonic distortion (THD). This variable-speed motor drive (VSMD) can save more electrical energy than a fixed-speed motor drive, given that both operate on the same load factor. Few of the small VSMDs have IPFC circuits to save on their production costs. A three-phase, inverter-fed induction motor drive (IMD) with a single-phase source and an active IPFC circuit was developed in order to study the impact of an experimental IPFC circuit. The focus of this study of an input PF-corrected VSMD was on the effects of the circuit on overall system efficiency and input PF. Empirical comparisons between the conventional bridge rectifier circuit and IPFC circuit, in terms of PF and efficiency as they relate to motor speed, were made. A steady-state model of the IMD, including a three-phase inverter and an active IPFC circuit, was developed to predict system performance. The analytical results were correlated to the experimental results obtained from a prototype, one-horsepower IMD using a constant volts-per-hertz (V/Hz) control strategy. The overall system performance of the IPFC circuit was better than without it in terms of harmonic contents and PF. The system efficiency, however, showed marginal inferiority over the IPFC circuit as the front-end IPFC circuit and the three-phase inverter were connected serially. It should be emphasized that the IMD, with the IPFC circuit, was desirable in order to utilize the generated electrical energy effectively, while minimizing the harmonic contamination.

Introduction

Emerging applications of fractional-horsepower IMDs—such as compressors, appliances, blowers, hand tools, and heating, ventilating, and air-conditioning (HVAC)—invoke the urgency of studying the effects of the IPFC on the VSMDs [1-5]. The necessity for efficient utilization of generated electrical energy is growing in significance in order to optimize the usage of utility power plant capacity. Moreover, awareness of minimizing harmonic contamination in the electric power line is rising due to the increased use of electronic equipment powered by an ac-to-dc bridge rectifier with large filter capacitors and/or a switch-mode power supply (SMPS).

One of the most active research and development areas in the power electronics field is VSMD [6-14]. As power semiconductor devices become cheaper, faster and more reliable, the use of energy-saving VSMDs in industry and residential applications has been increasing. VSMDs utilizing induction and dc motors make up the majority of industrial and domestic drives. Although these VSMDs require an initial investment and generate current harmonics, they provide significant improvements in performance such as better control, wider speed ranges, soft start, and enormous energy savings in various kinds of applications. The selection of VSMDs is an application-specific matter. There are many factors to be considered when selecting VSMD systems, including cost, output torque, speed ranges, performance, and power ratings.

The emerging requirement in VSMD applications for drawing near sinusoidal current from the utility and fewer harmonics being injected into the utility lines is the motivation for investigation of the PF-corrected motor drive system. The impact of IPFC on system efficiency and power converter ratings is to be studied for the high-volume but low-cost applications such as washers, dryers, refrigerators, freezers, hand tools, and process drives. The power ratings for most of these high-volume applications are less than one -horsepower.

All off-line VSMDs have rectifiers and storage capacitors in their front-ends to get dc voltage from an ac power source. This input circuitry lowers the PF of the VSMD systems and pollutes ac power systems. The PF is the ratio of real power in watts (W) to apparent power in volt-amperes (VA). The PF becomes unity when the input ac current and voltage are sinusoidal and in phase. In an off-line VSMD system, the input current is distorted and even out of phase with the input voltage, the power factor is less than unity, and less real power is transmitted to the load. However, the rms input current is increased due to the har-

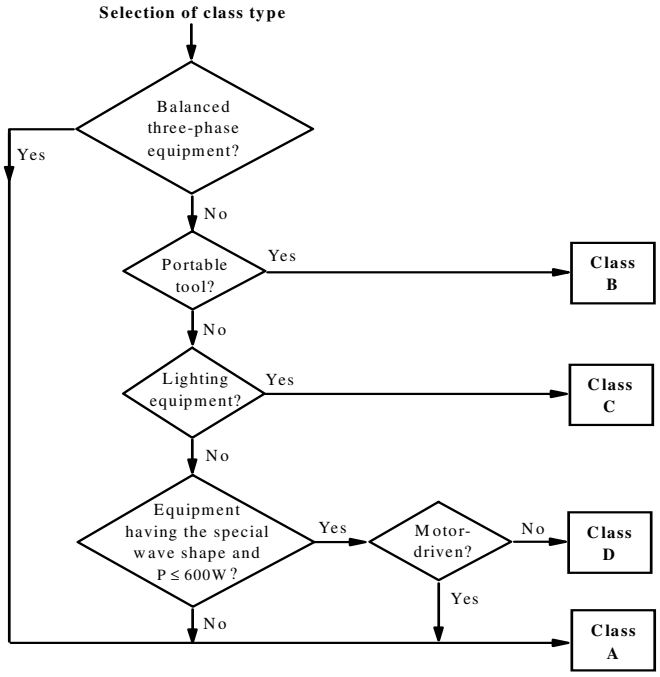
monic currents, plus the current required by the load must still be carried, thus requiring the wiring of the ac power system to be heavier and more expensive than necessary.

The most common problem with ac power systems is caused by electric motors operating in industries. The inductive component of the motors causes the ac current to lag the ac voltage. This results in a low power factor. Assuming the loads are linear, the power factor can be corrected to near unity by connecting a bank of capacitors across the ac power line. The low PF gives rise to a number of serious problems in VSMD systems. The size of the input fuses and circuit breakers of the input circuitry must be increased. The distorted input current waveform, which causes interference with other equipment, must be filtered to reduce the magnitude of the harmonic frequencies. Consequently, to increase the output power from ac power systems, it is necessary to correct the PF. This substantially reduces peak and rms input current and makes it possible to achieve higher output power.

With the proliferation of nonlinear loads such as SMPSs, standards agencies around the world are developing requirements for harmonic contents of the electronic power conversion systems to reduce the overall distortion on the main supply line. One of these standards is the IEC 1000-3-2 (same as EN 61000-3-2 published in 1995 and the latest version of IEC 555-2 published in 1982) [15] from the International Electrotechnical Commission (IEC) to set the limits for input harmonic currents in the electrical equipment. The standard describes general requirements for testing equipment as well as the limits and the practical implementations of the test. For the purpose of harmonic current limitation, the standard divides electrical equipment into four classes, as shown in Figure 1. Each class has different harmonic current limits. Any balanced, three-phase equipment or other electronic apparatus which do not fall into either Class B, C, or D will automatically be moved to Class A. To apply a Class D limit, the following two requirements should be satisfied:

- Input power should be less than 600W.
- The input current waveshape of each half cycle should be within the envelope shown in Figure 2 for at least 95% of the duration of each half period.

The center line in Figure 2 coincides with the peak value of the input current. The second requirement implies that the waveform, having a small peak outside the envelope, is considered to fall within the envelope. In Class D limits, for equipment with input power greater than 75W, relative limits (mA/W) should be applied; otherwise, absolute limits will be applied. The specified limits of the IEC 1000-3-2 standards are applicable to electrical equipment having an input current up to 16A per phase with nominal voltages of 230V with single-phase frequencies of 50 or 60Hz, and the harmonic currents of interest are from the 2nd to 40th harmonic.



Note. Motor-driven: Phase Angle Controlled

Figure 1. Flowchart for Class Determination of Electrical Equipment by IEC 1000-3-2 Standards

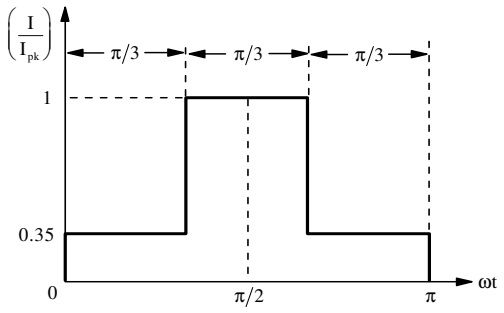


Figure 2. Class D Waveform Envelope

The appliance VSMDs fall into the Class A or D categories, depending on whether they use a phase-angle controlled VSMD, and their input power range is less than or greater than 600W. The VSMDs, which were investigated in this study, have front-end rectifier circuits to convert ac voltage into dc voltage. The ac input current of the VSMD has a pulse-type waveform, which falls into the Class D

envelope regardless of the magnitude of its input power because the pulse current is normalized based on its peak value. If the input power of a VSMD is over 600W, a Class A limit should be applied. Otherwise, the Class D limit will be applied. Therefore, in this study, only the Class A and D limits were employed to verify the effects of IPFC and IEC 1000-3-2 standards.

Single-Phase IPFC Topologies

The study of IPFC topologies is limited here to the single-phase version because most of the appliance VSMDs are powered by a single-phase utility source. The classification of single-phase, off-line IPFC topologies for VSMDs [16-19] is shown in Figure 3. Among these IPFC topologies, low frequency active, resonant and isolated types were not considered in this study. A passive IPFC [18] is more reliable than an active IPFC because no active devices are utilized. However, it has bulky capacitors and inductors operating at line frequency, and it is sensitive to the line frequency, line voltage, and load. Therefore, this method is not suitable for appliance drives. The most popular active IPFC method is the boost topology [16]. This topology is a universal solution for SMPS to small-motor drive applications. It has a smooth input current because an inductor is connected in series with the power source, showing a low level of conducted electromagnetic interference (EMI) noise. This topology has a high output voltage which is greater than the peak input voltage. The overload and start-up currents cannot be controlled in this topology because there is no series switch between the input and output path. Also, isolation between the input and output cannot be easily implemented.

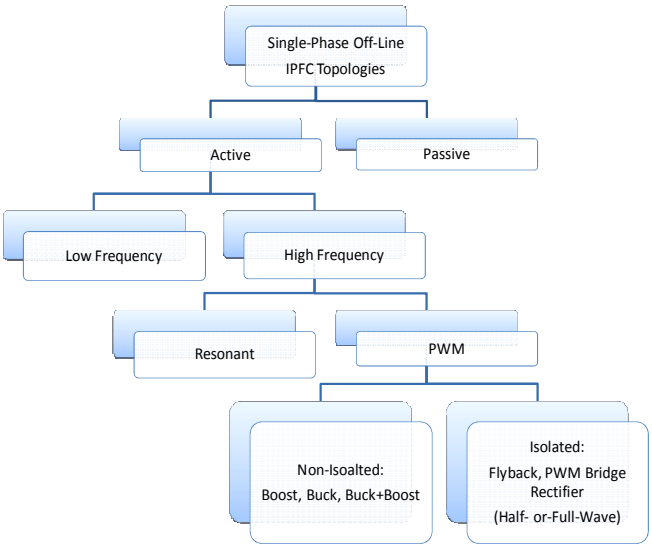


Figure 3. Classification of Single-Phase IPFC Topologies for Small VSMD Systems

The buck-type IPFC has lower output voltage than input voltage and it has a pulsating input current, which generates high harmonics in the power line. This circuit is not practical for low-line inputs because it does not draw the input current when input voltage is lower than output voltage. Therefore, it has a relatively low power factor compared to the boost IPFC circuit. The buck-type IPFC is suitable for charger applications due to its voltage step-down nature [17].

The SEPIC (single-ended primary inductor converter) IPFC circuit has a single power switch driven at high frequency, as with the boost IPFC topology, but it needs extra inductive and capacitive passive components for energy storage and transfer. The input current of SEPIC is smoothed by employing an inductor in series with the power source. This circuit can be easily modified to the isolated version. A cascaded converter, which has a buck circuit in the front and boost circuit in the second stage, is introduced by Singh & Singh [6]. The buck switch is turned on when the input voltage is below the output voltage. This causes the circuit to operate as a boost converter. When the input voltage is higher than the output voltage, the boost circuit is stopped and the buck circuit restarts. This converter can supply step-up or step-down outputs; thus, it can operate over a wide range of inputs. There is no inrush current due to the buck switch, which is in series with the power source, but it has a pulsating input current which requires more filtering.

Another non-isolated IPFC topology is the pulse width modulation (PWM) bridge rectifier. This topology can also supply step-up or step-down outputs, similar to the buck-boost circuit. The PWM bridge rectifier circuit needs two or four power switches to yield a unity power factor because it employs a half- or full-bridge configuration. It also needs a more complicated control circuit than the boost topology, but for high-power applications, it may be a good candidate.

Proposed IPFC-IMD System

The proposed IPFC-IMD system for this study is shown in Figure 4. Note that the IPFC circuit can be replaced with a single-phase diode rectifier bridge circuit for a comparative study. IPFC has both input current and voltage feedbacks in order to obtain the sinusoidal input current. The output voltage sensing circuit rejects the adverse effect of load variation on the dc link voltage. The inverter power circuit is made up of MOSFET devices and operates at 2.78kHz with PWM control. The control strategy is a constant V/Hz with the offset adjustment. In this study, the offset was fixed at a value equal to the rated stator resistive voltage drop. The drive had an inner rotor speed feedback

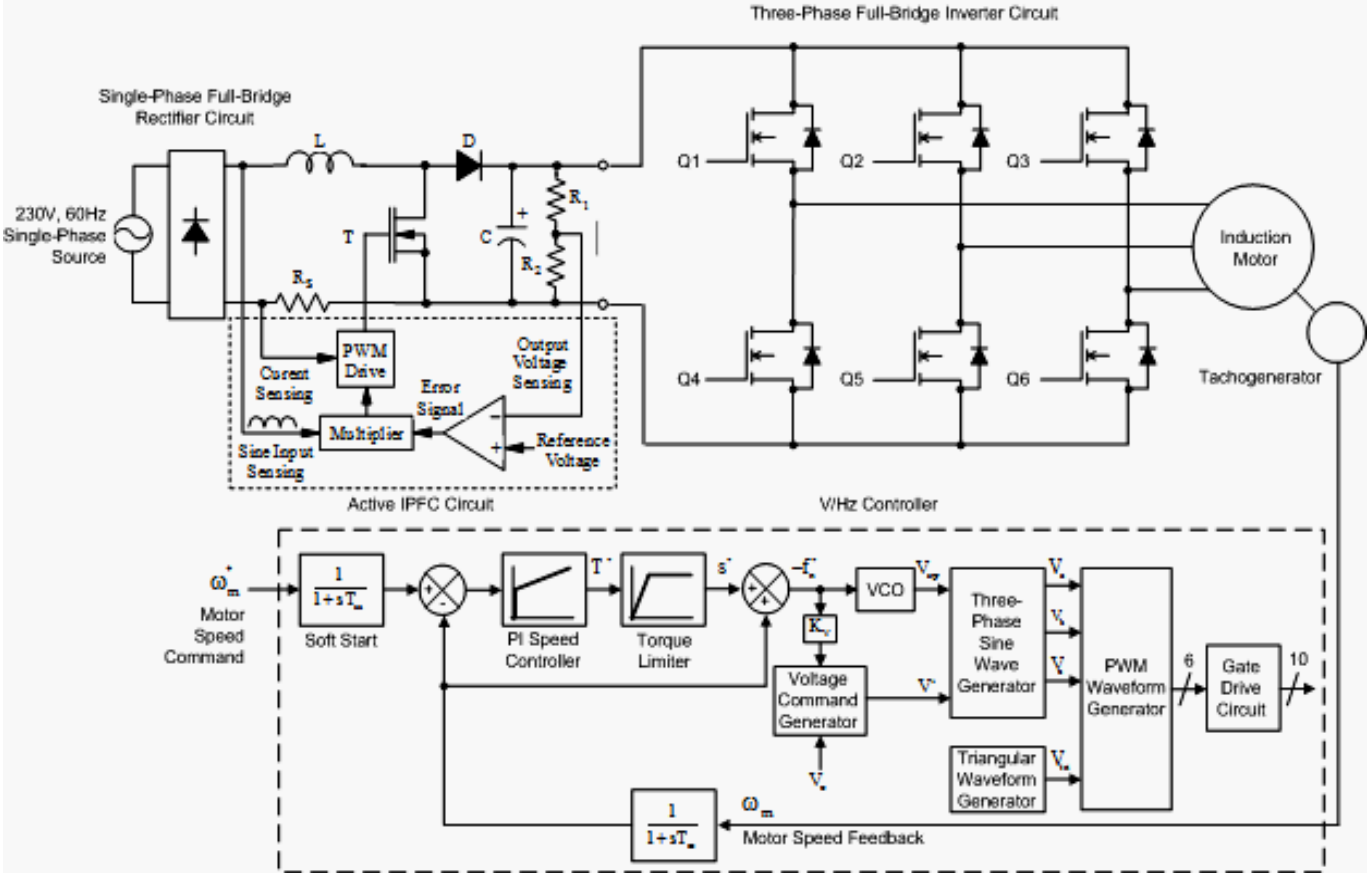


Figure 4. Proposed IPFC-IMD System

loop to control the slip speed. This limited the stator current effectively over the range of speed variation.

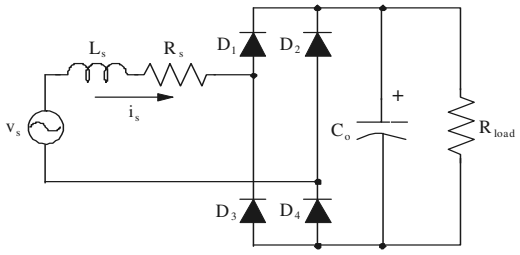
Principle of Operation of the Boost IPFC Circuit

The principle of operation of the boost IPFC circuit, which was selected for the VSMD system, is explained in this section. The predicted efficiency of the boost PFC pre-regulator was obtained with derived analytical equations and compared with experimental results. The harmonic contents in the input current of the boost PFC circuit were compared with the IEC 1000-3-2 standards [15], [20]. In a VSMD, the ac utility input voltage must be converted to dc with a rectifier circuit, as shown in Figure 4. This circuit has the advantages of simplicity, low cost, high reliability, and no need of control. However, it has the disadvantages of low PF due to the presence of rich harmonics in its current and a high peak-current magnitude, as shown in Figures 5 (a), (b), and (c). This relationship was obtained from the PSpice simulation of a single-phase diode bridge rectifier circuit and was normalized to the peak value.

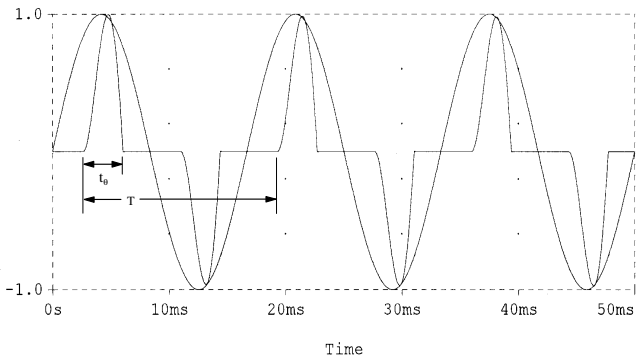
The input circuitry of an off-line VSMD consisted of rectifier diodes to convert ac into pulsating dc, and filter capacitors to smooth the pulsating dc voltage, as shown in Figure 4. This input circuitry presents rich harmonic currents to ac power systems that are quite different from motor loads because it appears as a nonlinear load to ac power systems. In the input circuitry, ac current pulses occur because the filter capacitor remains charged to nearly the peak value of the ac input voltage.

During most of each half cycle of the input voltage, the rectifier diodes remain reverse biased; thus, no current flows. Because the filter capacitors partly discharge during each half-cycle, the input voltage exceeds the capacitor voltage for a short time near the peak value of the input voltage. As the input voltage surpasses the capacitor voltage, the input current begins to flow abruptly into the capacitor. After the capacitor is charged almost to the peak value of the

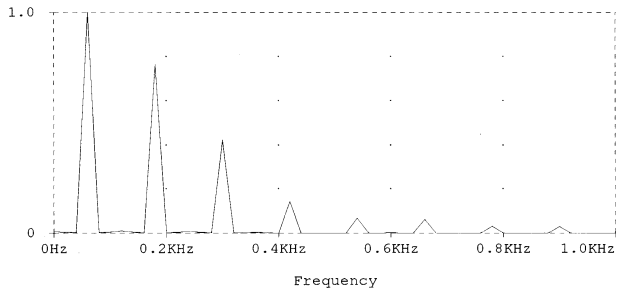
input voltage and the input voltage begins to decrease, the input current falls to zero. Also, it causes overheating of the power lines and distribution transformers. Under extreme conditions, other sensitive electronic equipment connected to the same power line can be affected by noise related to electromagnetic interference (EMI).



a) A Single-Phase Diode Rectifier Circuit with Capacitor



b) Normalized Input ac Voltage, v_s and Current, i_s



c) Normalized Harmonic Spectrum of Current i_s

Figure 5. Analysis of Current Harmonic Contents in the Diode Bridge Rectifier Circuit with Capacitor by Simulation

As required by various standards, the line harmonics produced by a VSMD must be below certain limits, which increase the input PF. The high PF is desirable to both the user and the utility company because it is possible to get maximum power from an ac service outlet and to utilize the generated power efficiently and cleanly. It is also possible to reduce the wiring and power transformer losses in the utility network with high PF. With increasing demand for more power and better power quality from a standard power line, the IPFC circuit will become an integral part of VSMDs in the near future.

The boost IPFC circuit is an economical solution to the need for complying with the regulations. It can be implemented with a dedicated single-chip controller; therefore, the circuit becomes relatively simple with a minimum number of components. The boost inductor in the boost IPFC circuit is in series with the ac power line; thus, the input current does not pulsate and the conducted EMI at the line is minimized. This allows the size of the EMI filter and the conductors in the input circuit to be reduced. This topology inherently accepts the wide input voltage range without an input voltage selector switch. For example, the UC3854 PF controller chip from Texas Instruments [21] accepts an input voltage of 75 – 275VAC and a frequency of 50–400Hz. It cannot limit overcurrent at start-up or fault conditions because there is no switch between the line and the output.

The output voltage of a boost IPFC circuit should be higher than the peak value of the maximum input voltage. Even though this is a simple topology, it must be designed to handle the same power as the main power converter. Only the single-phase boost IPFC circuit operating in the continuous-inductor-current mode was addressed in this study. The simplified block diagram of the boost IPFC circuit is shown in Figure 4. This circuit has two control loops. One is the fast-acting internal current loop, which defines the input current shape to be sinusoidal and places it in phase with the input voltage. The other is the external voltage loop, which regulates the output dc voltage. The voltage loop should not react to the 120Hz rectified mains variations, so its bandwidth was lowered to 10 to 20Hz. The current loop usually has a bandwidth frequency of less than one tenth of the switching frequency.

The principle of operation of the boost IPFC is as follows: the rectified sinusoidal input voltage goes to a multiplier circuit, providing a current reference to the multiplier and a feedforward signal proportional to the rms value of the line voltage. The filtered dc output voltage of the boost IPFC is compared to a reference voltage and amplified. The error amplifier senses the variations between the output voltage and the fixed dc reference voltage. The error signal is then applied to the multiplier. The multiplier's output follows the shape of the input ac voltage, with an average value inversely proportional to the rms value of the ac input voltage. This signal is compared to the sensed current signal in a PWM circuit. The inductor current waveform follows the shape of

the rectified ac line voltage. The gate drive signal controls the inductor current amplitude and maintains the constant output voltage.

Derivation of the Steady-State IPFC-IMD System Model for Analysis

Steady-state loss models of the induction motor, load, inverter, IPFC circuit, and bridge rectifier were developed and a procedure to compute various subsystem variables is presented in this section.

The load and its requirements are known and, hence, they constitute the starting point for the steady-state performance computation. Using the rotor speed and the load power with the inverter output voltage equation, induction motor equations, and load equations, the overall system equations were assembled. What follows is the solution of the system equation iteratively for the slip, stator frequency and all other variables for each speed with a specific load.

As the stator phase current was given, the inverter losses could be computed with switching and conduction loss equations. The input power to the inverter could be calculated with the inverter losses combined with the induction motor input power. The sum of inverter input power and the IPFC circuit losses yields the input power from the ac mains supply. The solution of the input power leads to a complete solution of the steady-state performance of the IPFC-IMD system.

Bridge Rectifier

Only the diode conduction losses were considered. The conduction losses in a single-phase rectifier bridge, P_{br} , are given by Equation (1),

$$P_{br} = 2V_d I_{in} = 2V_d \cdot \frac{P_{in}}{V_{in}} \tag{1}$$

where V_d is the forward diode voltage drop, I_{in} is the ac input current, V_{in} is the ac input voltage, and P_{in} is the ac input power from the ac mains supply.

IPFC Circuit

The IPFC circuit has a single power device with a forward diode in the boost configuration. The peak current in the boost inductor in terms of the ac input current, I_{in}, is

$$I_p = \sqrt{2} I_{in} = \frac{\sqrt{2} P_{in}}{V_{in}} \tag{2}$$

The IPFC circuit is designed to operate with 10% ripple current in the boost inductor. The current in the power switching device is,

$$I_{sw} = \sqrt{\frac{I_p^2}{2} - I_d^2} \tag{3}$$

where I_d is the boost diode current given by,

$$I_d = I_p \sqrt{\frac{4V_o}{3\pi V_{pk}}} \tag{4}$$

and where V_o is the dc output voltage of the IPFC circuit and V_{pk} is the peak rectified ac line voltage.

The losses in the boost switch are modeled as

$$P_{sw} = I_{sw}\left[\frac{1}{2} V_{pk} f_c \left(t_{rp} + t_{fp}\right) + I_{SW} R_{ds}(on)\right] \tag{5}$$

where t_{rp} and t_{fp} are the rise and fall times of the boost power switch, respectively.

$R_{ds}(on)$ is the on-state drain-to-source resistance of the MOSFET power device and f_c is the carrier frequency of the IPFC circuit.

The losses in the boost diode are

$$P_d = I_d\left(\frac{1}{2} V_{dc} f_c t_{rrd} + V_d\right) \tag{6}$$

where t_{rrd} is the reverse recovery time of the boost diode in the IPFC circuit.

The losses in the boost inductor are

$$P_{ind} = R_{dc} I_{in}^2 \tag{7}$$

where R_{dc} is the dc resistance of the inductor.

The losses, P_{bripfc}, in the diode bridge rectifier when the IPFC circuit is used are given by

$$P_{bripfc} = 2I_{ave} V_d = \frac{2}{\pi} I_{pk} V_d \tag{8}$$

where I_{ave} is the average current in the single-phase bridge rectifier and V_d is the forward conduction voltage drop in the diodes.

The total losses in the IPFC circuit, including the controller power supply losses, P_{ps}, is obtained as

$$P_{ipfc} = P_{bripfc} + P_{sw} + P_d + P_{ind} + P_{ps} \tag{9}$$

Inverter

The inverter output phase voltage is designed as a function of stator frequency command of the induction motor and given as

$$V_i = V_{as} = V_{of} + k_{vf} \cdot f_s \tag{10}$$

where V_{of} is the offset voltage given by

$$V_{of} = I_b R_s \tag{11}$$

The constant, k_{vf}, is given by

$$k_{vf} = \frac{V_b - V_{of}}{f_b} \tag{12}$$

where I_b is the base stator phase current, V_b is the base stator phase voltage, and f_b is the base stator frequency.

The inverter switching loss, P_{isw}, and conduction loss, P_{icon} , are modeled as

$$P_{isw} = m\left[\frac{1}{2} V_{dc} I_s f_{sw} \left(t_r + t_f + t_{rr}\right)\right] \tag{13}$$

$$P_{icon} = m I_s^2 R_{ds}(on) \tag{14}$$

where t_r and t_f are the rise and fall times of the power devices, respectively, and t_{rr} is the reverse recovery time of the freewheeling diodes. And, f_{sw} is the inverter switching frequency, $R_{ds}(on)$ is the on-state resistance of the MOSFET power device, and V_{dc} is the dc link voltage input to the inverter.

Induction Motor

A single-phase equivalent circuit of the three-phase induction motor is shown in Figure 6 [22], [23]. The loop voltage equations from the equivalent circuit are

$$V_{as} = \left(R_s + j\omega_s L_{ls}\right) I_s + Z_o I_o \tag{15}$$

$$0 = \left(\frac{R_r}{s} + j\omega_s L_{lr}\right) I_r + Z_o I_o \tag{16}$$

where

$$I_s = I_r + I_o \tag{17}$$

$$Z_o = j\frac{\omega_s L_m R_c}{\left(R_c + j\omega_s L_m\right)} \tag{18}$$

and where I_s, I_r, and I_o are the stator, rotor, and magnetizing branch currents, respectively. V_{as} is the stator phase voltage, w_s is the stator angular speed, R_s is the stator phase resistance, and R_r is the stator referred rotor phase resistance. L_m, L_{ls}, and L_{lr} are the magnetizing, stator leakage, and stator referred rotor leakage inductances per phase, respectively, and s is the slip given by

$$s = \frac{\omega_s - \omega_r}{\omega_s} = 1 - \frac{\omega_r}{\omega_s} = 1 - \frac{P}{2} \cdot \frac{\omega_m}{\omega_s} = 1 - \frac{nP}{120 f_s} \tag{19}$$

where w_m and w_r are rotor mechanical and electrical angular speed, respectively, N is the rotor speed in r/min, P is the number of poles, and f_s is the supply stator frequency.

The mechanical power developed in the rotor, P_m, for the m-phase machine is given by

$$P_m = m I_r^2 R_r \cdot \frac{\left(1 - s\right)}{s} \tag{20}$$

where m is the number of phases (three) in this study.

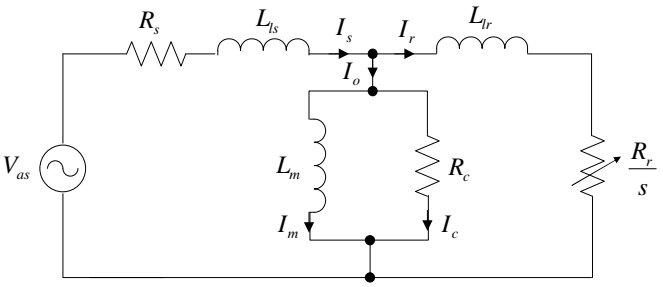


Figure 6. Single-Phase Equivalent Circuit of the Three-Phase Induction Motor

Load

The load power, P_o, is related to the induction motor output in steady-state by

$$P_o = P_m - P_{fw} \tag{21}$$

where P_{fw} is the friction and windage losses.

In general, the output of any load is given as

$$P_o = P_b\left(\frac{n}{n_b}\right)^k \tag{22}$$

where P_b is the base power, n_b is the base speed in r/min and k is 1, 2, and 3 for constant, frictional, and fan-type loads, respectively. Note that P_{fw} is the function of motor speed, n.

Discussion of Experimental Results

From the experimental data containing the friction and windage losses, the parameters of the induction and dc machines were calculated and, in conjunction with other measurements, the induction motor output was determined for each operating point. Then, the system and induction motor efficiencies, system input PF, system line current, motor currents, and IPFC circuit efficiencies were calculated from the empirical data.

The speed of the induction motor was varied from 500 r/min to 3,000 r/min (0.87 p.u.), and the output power at the base speed (3,450 r/min) was 1 hp. The empirical data were obtained for the system with and without the IPFC circuit, and by keeping the input system voltage at 230V.

Input Current Harmonics in the Boost IPFC Preregulator

The sample input current waveform and its harmonic contents of the prototype 2kW IPFC preregulator with a 1400W load are shown in Figure 7. The steady-state harmonics were measured by Fast Fourier Transformation (FFT) with the rectangular windowing function. The input ac current closely followed the sinusoidal voltage waveform, as designed. The PF of this operating point was calculated as 99% using the following equations:

$$Power\ \ Factor = \frac{Real\ Power}{Apparent\ Power} = \frac{V_{rms} \cdot I_1 \cdot \cos\phi}{V_{rms} \cdot I_{rms}} = \frac{I_1}{I_{rms}} \cdot \cos\phi \tag{23}$$

$$I_{rms} = \sqrt{I_1^2 + I_3^2 + \cdots + I_n^2} \tag{24}$$

where V_{rms} is the ac input rms voltage, I_{rms} is the input ac current, I_1 is the fundamental component of I_{rms} and *cosf* is the phase angle between input ac voltage and the fundamental current. The harmonic spectra of the input current with the IPFC circuit are shown in Figure 7. The input ac current closely follows the sinusoidal voltage waveform as designed. The comparison of the measured input current harmonic spectra magnitude with the modified IEC 1000-3-2 Class A limit is shown in Figure 8. The harmonic spectra of the input current with the IPFC circuit are vastly improved compared with one in the bridge rectifier circuit with a capacitor. This validates the effectiveness of the IPFC.

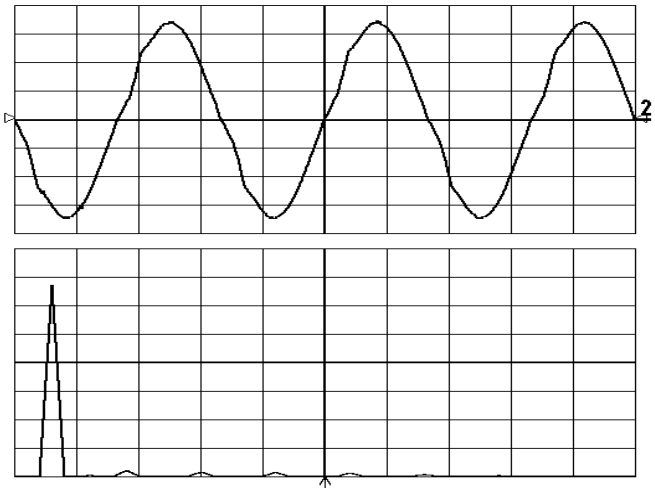


Figure 7. Experimental Waveforms of the 2kW PFC Preregulator with 1.4kW Load (top) Input Current (5A/div, 5ms/div) (bottom) Input Current Harmonic Spectra (2.5A/div, 0.1kHz/div)

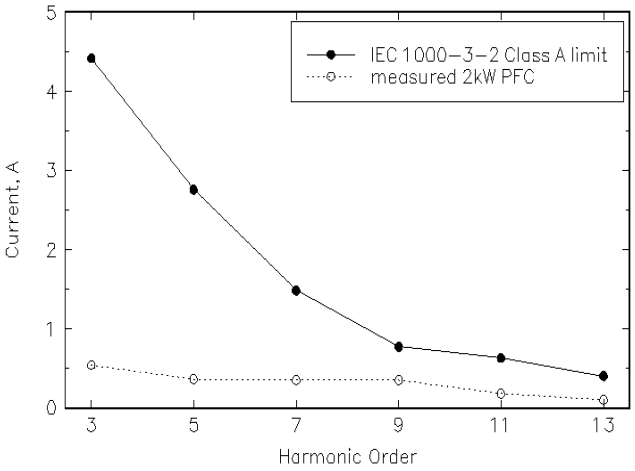


Figure 8. Comparison of Measured Input Current Harmonic Spectra from Figure 7 with Modified IEC 1000-3-2 Class A Harmonic Current Limit

Experimental waveforms of the system input current and induction motor stator current at 1 p.u. speed and load torque are shown in Figures 9 and 10, for both the bridge rectifier- and IPFC-based VSMD systems along with their frequency spectra. The IPFC-IMD system was free of harmonics in the system input current. The induction motor stator currents were practically the same with minor variations in their frequency spectra. The speed variation hardly affected these waveforms.

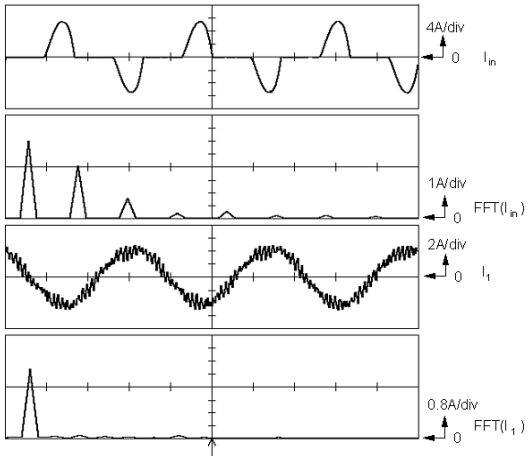


Figure 9. System ac Input Current (top) and Motor Stator Current (bottom) and their FFT with Diode Bridge Rectifier Front-end (Horizontal/div: Currents = 5ms, FFT = 100Hz)

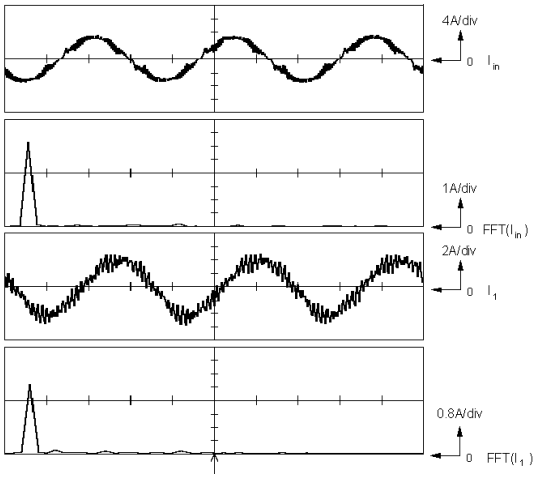


Figure 10. System ac Input Current (top) and Motor Stator Current (bottom) and their FFT with IPFC Circuit (Horizontal/div: Currents = 5ms, FFT = 100Hz)

Efficiencies of the IPFC Circuit and the IMD System

In Figure 11, the efficiency of the 2kW IPFC circuit employed in this study remained level above 95% over the entire output power range. The predicted efficiency matched closely with the measured one over the entire power range. This validation of the derived loss models has practical usefulness in estimating losses in the boost IPFC preregulator.

The system input PF, input current, and overall IMD system efficiency versus motor speed for systems either with or without the IPFC preregulator are shown in Figures 12(a), (b), and (c) for the friction load. The IPFC-based IMD showed a higher input PF over the entire speed range than one with a non-IPFC system. Hence, the IPFC-IMD system required lower input current to generate the same output compared with a non-IPFC system. The benefit of requiring less input current was noticeable over 0.4 p.u. speed. The non-IPFC system showed higher system efficiency up to 0.75 p.u. speed, but the IPFC-based system showed higher system efficiency beyond that speed with a friction load. This is attributed to the fact that the stator current decreases with the decreasing stator voltage of the non-IPFC system. The non-IPFC system efficiency was approximately 2 to 4% higher than that of the IPFC-based system.

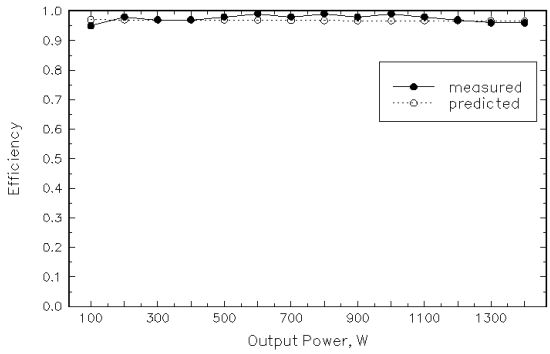
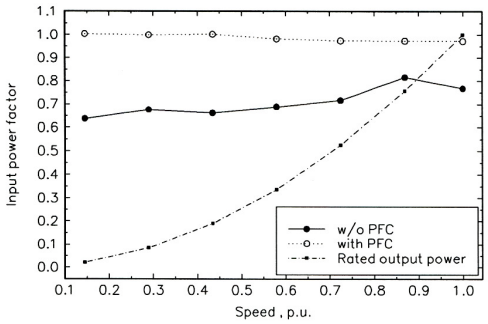
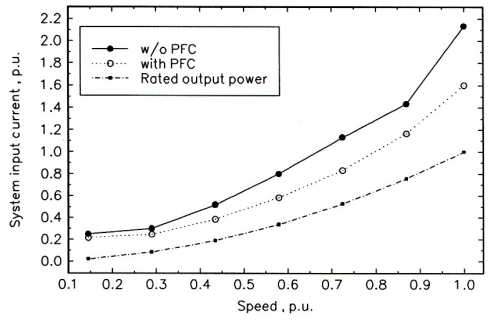


Figure 11. Measured and Predicted Efficiencies for the Developed 2kW Boost IPFC Preregulator

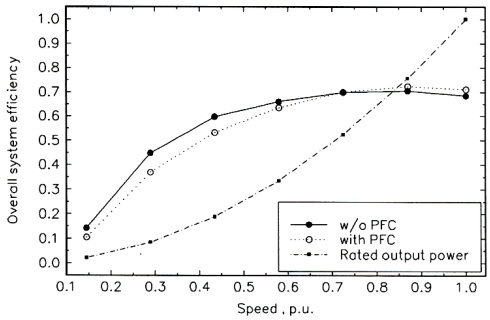


a) System Input PF



b) System Input Current

Figure 12. Input PF, Current, and System Efficiency with and without IPFC with Friction Load (continued on next page)



c) Overall system efficiency

Figure 12 (continued). Input PF, Current, and System Efficiency with and without IPFC with Friction Load

The effect of IPFC to the three-phase inverter performance in terms of output voltage and current are shown in Figures 13(a) and (b). The IPFC-IMD system showed higher output voltage than the one with the non-IPFC system because of the tight output voltage regulation of the IPFC control circuit. The inverter needed less current output to drive the IMD to the same speed.

However, the IPFC benefits from the efficiency of the induction motor slightly over 0.6 p.u. speed. The system and motor efficiencies were very poor for speeds lower than 0.3 p.u., as the output was very small in this region and the losses were many times that of the output in that speed range. The usual variation of speed range was 0.4 to 1 p.u. for the friction load; hence, the low-speed operation with low efficiency may not be of immense importance.

Conclusions

The system steady-state model for both the bridge rectifier- and IPFC-based IMD were formulated, and a steady-state computational procedure was developed. The model was experimentally verified with a 1-hp laboratory prototype IPFC-IMD system and was found to be fairly accurate.

A comparison between the non-IPFC- and IPFC-based systems was made for the friction type load. The non-IPFC system was preferable in terms of system efficiency; the IPFC-IMD system may not be quite as attractive due to additional cost, however, the IPFC-based system was highly preferable for the minimum input harmonics and maximum PF.

Acknowledgements

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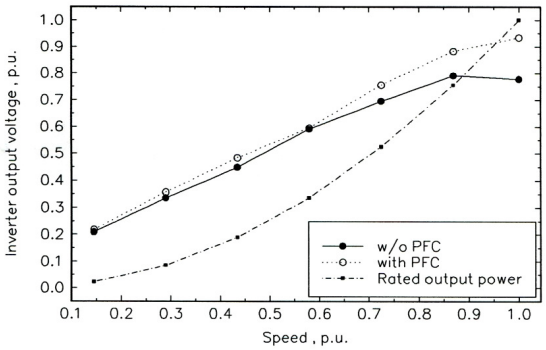
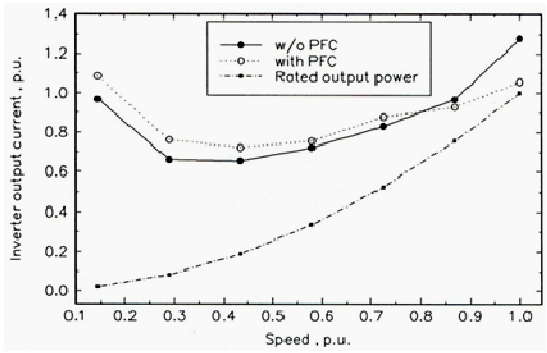
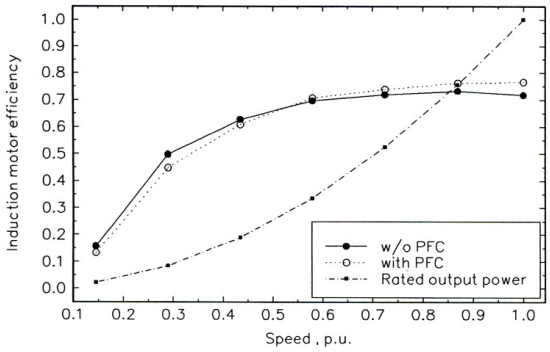


a) Inverter Output Voltage



b) Inverter Output Current



c) Induction Motor Efficiency

Figure 13. Inverter Output Voltage, Current, and Induction Motor Efficiency with and without IPFC for the IMD System with Friction Load

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Offices. *IEEE Transactions on Power Delivery*, 20 (3), 2257-2263.
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